

LQ025Q3DW02 TFT-LCD Module

Product Specification

October 2007

High Brightness, High Contrast LCD Module
with Wide Viewing Angle and Normally Black
display. Full Specifications Listing

| | | |
|------------------------------------|--|--|
| PREPARED BY: <i>H. Toyota</i> | SHARP | SPEC No. LD-19X15A |
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DEVICE SPECIFICATION FOR

TFT-LCD module

 MODEL No. LQ025Q3DW02

These parts have corresponded with the RoHS directive.

CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED

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1. Applicable Scope

This specification is applicable to TFT-LCD Module “LQ025Q3DW02”.

2. General Description

This module is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver IC, Input FPC, a back light unit.

Graphics and texts can be displayed on a 320 × RGB × 240 dots panel with about 262k colors by supplying 18bit data signals (6bit × RGB), four timing signals, 3wires 9bit serial interface signals, logic (Typ. +3.3V), analog (Typ. +3.3V) supply voltages for TFT-LCD panel driving and supply voltage for back light.

3. Mechanical (Physical) Specifications

| Item | Specifications | Unit |
|---------------------------|--------------------------------|-------|
| Screen size | 6.3(2.5" type) diagonal | cm |
| Active area | 49.92 (H) × 37.44 (V) | mm |
| Pixel format | 320 (H) × 240 (V) | pixel |
| | 1 Pixel = R+G+B dots | - |
| Pixel pitch | 0.156 (H) × 0.156(V) | mm |
| Pixel configuration | R,G,B vertical stripes | - |
| Display mode | Normally black | - |
| Unit outline dimensions * | 56.8(W) × 48.8 (H) × Max3.5(D) | mm |
| Mass | Max.25 | g |
| Surface treatment | Anti glare | - |

*The above-mentioned table indicates module sizes without some projections and FPC.

For detailed measurements and tolerances, please refer to 17. Outline Dimensions.

4. Input Terminal Names and Functions

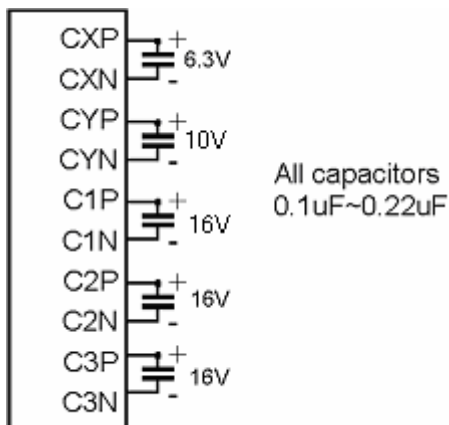
Recommendation CN : [HIROSE] FH26G-67S-0.3SHBW(05)

| Pin No. | Symbol | I/O | Description | Remarks |
|---------|-------------------|-----|--|---------|
| 1 | LED_C (-) | - | Power supply for LED (Low voltage) | |
| 2 | LED_A(+) | - | Power supply for LED (High voltage) | |
| 3 | DGND1 | - | Digital Ground | |
| 4 | NC | - | Not connected | Note 1 |
| 5 | NC | - | Not connected | Note 1 |
| 6 | NC | - | Not connected | Note 1 |
| 7 | NC | - | Not connected | Note 1 |
| 8 | AGND1 | - | Analog Ground | |
| 9 | V _{GH} | - | Connect to a Stabilizing capacitor | Note 3 |
| 10 | C2P | - | Connect a Booster capacitor to C2N | Note 2 |
| 11 | C2N | - | Connect a Booster capacitor to C2P | |
| 12 | C1P | - | Connect a Booster capacitor to C1N | |
| 13 | C1N | - | Connect a Booster capacitor to C1P | |
| 14 | V _{GL} | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 15 | C3P | - | Connect a Booster capacitor to C3N | Note 2 |
| 16 | C3N | - | Connect a Booster capacitor to C3P | |
| 17 | AGND2 | - | Analog Ground | |
| 18 | V _{CIX2} | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 19 | CYP | - | Connect a Booster capacitor to CYN | Note 2 |
| 20 | CYN | - | Connect a Booster capacitor to CYP | |
| 21 | V _{Cl} | - | 3.3V(Booster input voltage pin) | Note 3 |
| 22 | NC | - | Not connected | Note 1 |
| 23 | AGND3 | - | Analog Ground | |
| 24 | V _{CIM} | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 25 | CXP | - | Connect a Booster capacitor to CXN | Note 2 |
| 26 | CXN | - | Connect a Booster capacitor to CXP | |
| 27 | TEST | O | TEST | Note 1 |
| 28 | RESB | I | System reset | |
| 29 | DGND2 | - | Digital Ground | |
| 30 | V _{DDIO} | - | 3.3V(Voltage input pin for logic I/O) | |
| 31 | V _{CORE} | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 32 | DGND3 | - | Digital Ground | |
| 33 | SHUT | I | Sleep mode control | |
| 34 | CSB | I | Chip select pin of serial interface | |
| 35 | SDI | I | Data input pin in serial mode | |
| 36 | SCK | I | Clock input pin in serial mode | |
| 37 | V _{DROP} | - | Connect a Stabilizing capacitor | |
| 38 | DEN | I | Display enable | |
| 39 | B5 | I | BLUE data signal(MSB) | |
| 40 | B4 | I | BLUE data signal | |
| 41 | B3 | I | BLUE data signal | |

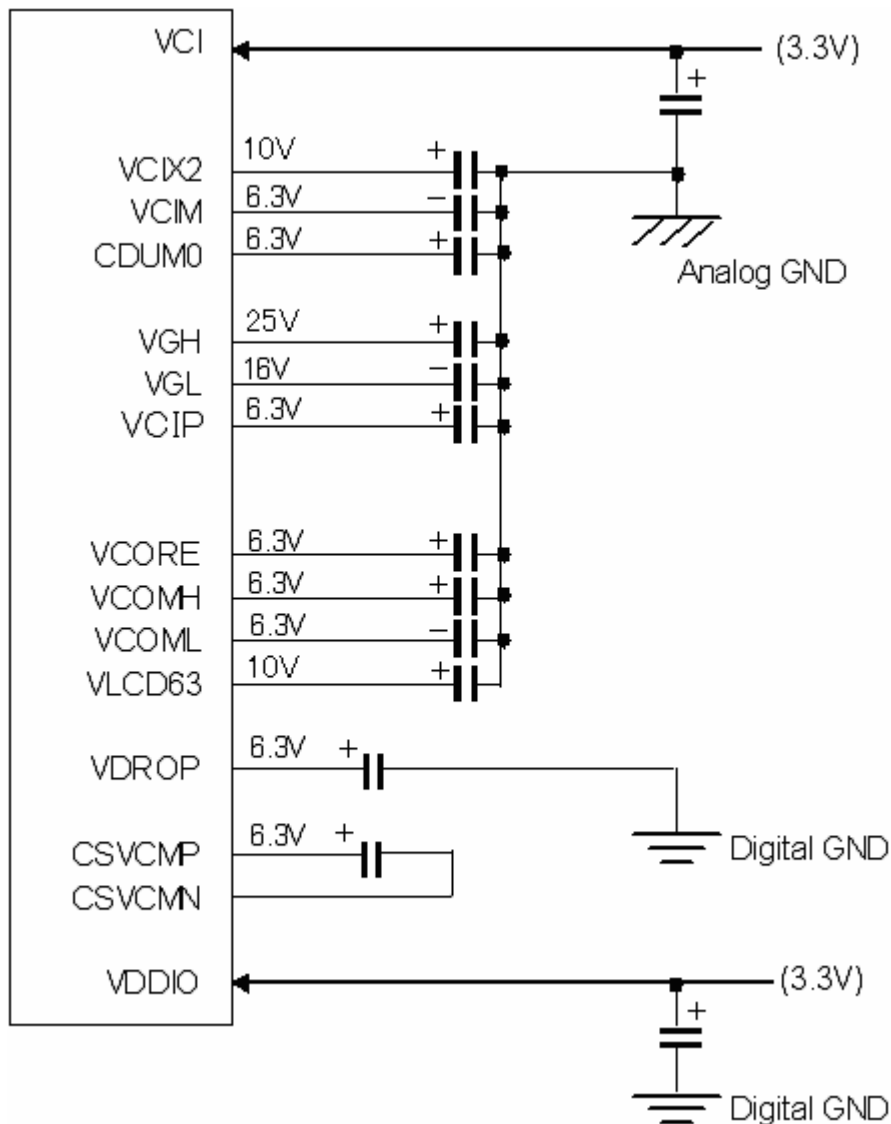
| Pin No. | Symbol | I/O | Description | Remarks |
|---------|--------------------|-----|---|---------|
| 42 | B2 | I | BLUE data signal | |
| 43 | B1 | I | BLUE data signal | |
| 44 | B0 | I | BLUE data signal(LSB) | |
| 45 | G5 | I | GREEN data signal(MSB) | |
| 46 | G4 | I | GREEN data signal | |
| 47 | G3 | I | GREEN data signal | |
| 48 | G2 | I | GREEN data signal | |
| 49 | G1 | I | GREEN data signal | |
| 50 | G0 | I | GREEN data signal(LSB) | |
| 51 | R5 | I | RED data signal(MSB) | |
| 52 | R4 | I | RED data signal | |
| 53 | R3 | I | RED data signal | |
| 54 | R2 | I | RED data signal | |
| 55 | R1 | I | RED data signal | |
| 56 | R0 | I | RED data signal(LSB) | |
| 57 | VSYNC | I | Frame synchronization signal | |
| 58 | HSYNC | I | Line synchronization signal | |
| 59 | DOTCLK | I | Dot-clock signal | |
| 60 | CDUM0 | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 61 | DGND4 | - | Digital Ground | |
| 62 | V _{LCD63} | - | Connect a Stabilizing capacitor to GND | Note 3 |
| 63 | V _{COMH} | - | Connect a Stabilizing capacitor to GND | |
| 64 | V _{COML} | - | Connect a Stabilizing capacitor to GND | |
| 65 | DGND5 | - | Digital Ground | |
| 66 | CSVCMN | - | Connect a Stabilizing capacitor to CSVCMN | Note 3 |
| 67 | CSVCMN | - | Connect a Stabilizing capacitor to CSVCMN | |

Note 1) this pin should be opened.

Note 2) Booster Capacitors



Note 3) Stabilization and charge sharing Capacitors



Remark :

Capacitor for VCIX2=2.2uF

All other capacitors 1.0uF ~ 2.2uF

(2.2uF is preferred for better display quality and power consumption)

5. Absolute Maximum Ratings

| Item | Symbol | Conditions | Rated value | Unit | Remarks |
|--------------------------------|-------------------|--------------------------|-------------------------------|------|---------|
| Input voltage | VI | Ta = 25°C | -0.3 ~ V _{DDIO} +0.3 | V | Note 1 |
| Logic I/O power supply voltage | V _{DDIO} | Ta = 25°C | -0.3 ~ +4.0 | V | |
| Analog power supply voltage | V _{CI} | Ta = 25°C | AGND-0.3 ~ +5.0 | V | |
| Temperature for storage | Tstg | - | -25 ~ +70 | °C | Note 2 |
| Temperature for operation | Topp | - | -10 ~ +60 | °C | Note 3 |
| LED input electric current | I _{LED} | T _{aLED} = 25°C | 35 | mA | |
| LED electricity consumption | P _{LED} | T _{aLED} = 25°C | 123 | mW | Note 4 |

Note 1) RESB, SHUT, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

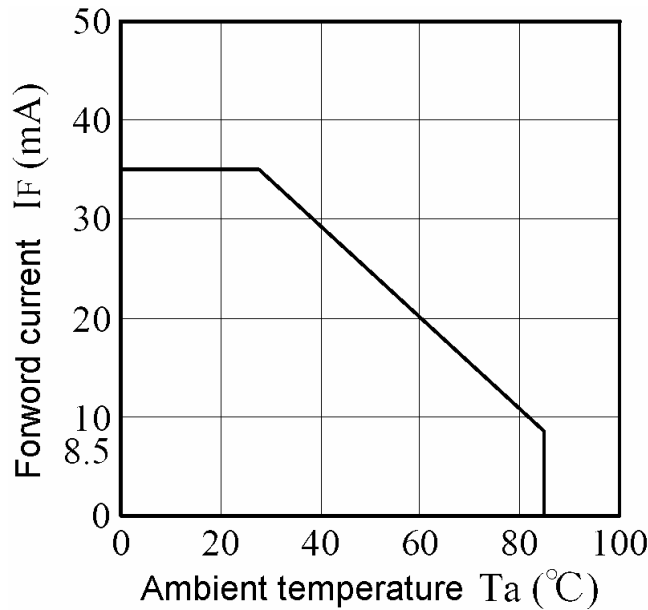
Note 2) Humidity: 95%RH Max. (Ta 40°C)

Maximum bulb temperature under 39°C (Ta>40°C) See to it that no dew will be condensed.

Note 3) Panel surface temperature prescribes.

Note 4) Power consumption of one LED (Ta_{LED} = 25°C). (use 4 pieces LED)

Ambient temperature and the maximum input are fulfilling the following operating conditions.



Ambient temperature of LED and the maximum input

6. Electrical Characteristics

6-1. TFT LCD Panel Driving

Ta = 25°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|------------------------------------|------------|-------------------|----------------|------|----------------|---------|---------|
| Logic I/O power supply | DC voltage | V_{DDIO} | +3.0 | +3.3 | +3.6 | V | |
| | DC Current | I_{VDDIO} | - | 0.15 | 0.30 | mA | Note 1 |
| Analog power supply | DC voltage | V_{CI} | +3.0 | +3.3 | +3.6 | V | |
| | DC Current | I_{VCI} | - | 7 | 10 | mA | Note 1 |
| Permissive input Ripple voltage | | $V_{RFVDDIO}$ | - | - | 100 | mVp-p | Note 2 |
| | | V_{RFVCI} | - | - | 100 | mVp-p | Note 2 |
| Logic Input Voltage | High | V_{IH} | $0.8 V_{DDIO}$ | - | V_{DDIO} | V | Note 3 |
| | Low | V_{IL} | 0 | - | $0.2 V_{DDIO}$ | V | Note 3 |
| Logic input Current | | I_{IH} / I_{IL} | -1 | - | 1 | μA | Note 3 |

Note 1) $V_{DDIO} = V_{CI} = +3.3V$ Current situation for I_{VDDIO} : Black & White checker flag patternCurrent situation for I_{CI} : All white patternNote 2) $V_{DDIO} = V_{CI} = +3.3V$

Note 3) RESB, SHUT, CSB, SDI, SCK, DEN, B5~B0, G5~G0, R5~R0, VSYNC, HSYNC, DOTCLK

6-2. Register Setting

| Reg. # | Register | Data (Gamma 2.2) | Remark |
|--------|-----------------------------|---------------------|--------|
| R01 h | Driver output control | 0xEF h | Note1 |
| R02 h | LCD drive AC control | 0300h | |
| R03 h | Power control (1) | 7A7E h | |
| R0B h | Frame cycle control | DC00 h | |
| R0C h | Power control (2) | 0005 h | |
| R0D h | Power control (3) | 0002 h | |
| R0E h | Power control (4) | 2C00 h | |
| R0F h | Gate scan starting Position | 0000 h | |
| R16 h | Horizontal Porch | 9F86 h | Note2 |
| R17 h | Vertical Porch | 0002 h | Note3 |
| R1E h | Power control (5) | 0000 h | |
| R28 h | Power control (6) | 0006 h | |
| R2C h | Power control (7) | C88C h | |
| R2E h | Gamma control (1) | B945 h | |
| R30 h | Gamma control (2) | 0004 h | |
| R31 h | Gamma control (3) | 0407 h | |
| R32 h | Gamma control (4) | 0002 h | |
| R33 h | Gamma control (5) | 0107 h | |
| R34 h | Gamma control (6) | 0507 h | |
| R35 h | Gamma control (7) | 0003 h | |
| R36 h | Gamma control (8) | 0307 h | |
| R37 h | Gamma control (9) | 0704 h | |
| R3A h | Gamma control (10) | 1F09 h | |
| R3B h | Gamma control (11) | 090E h | |

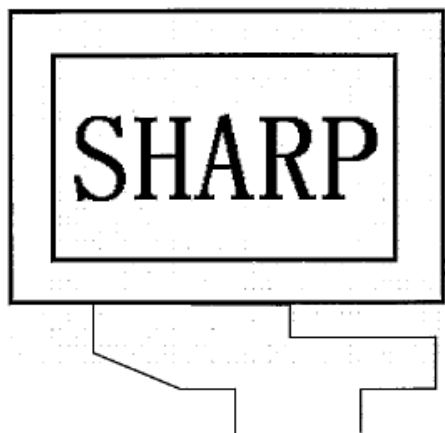
Note 1)

Driver Output Control (R01h)(POR=0xEFh)

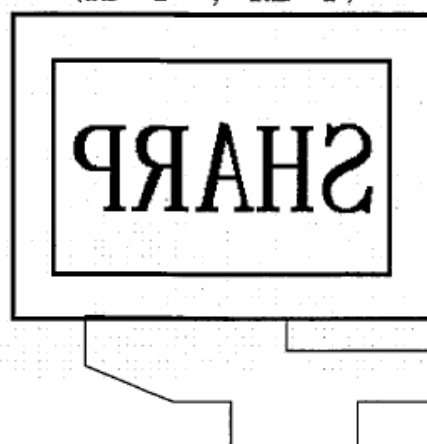
| | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W | 1 | 0 | 0 | 1 | 0 | 1 | 0 | TB | RL | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| POR | 0 | 0 | 0 | 0 | 0 | 1 | 0 | x | x | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

Vertical and Horizontal inversion function(TB , RL)

(TB="1" , RL="0")



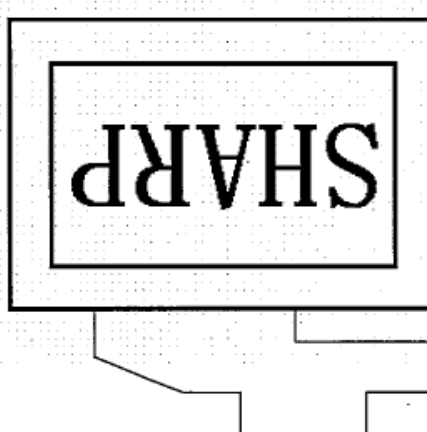
(TB="1" , RL="1")



(TB="0" , RL="0")



(TB="0" , RL="1")



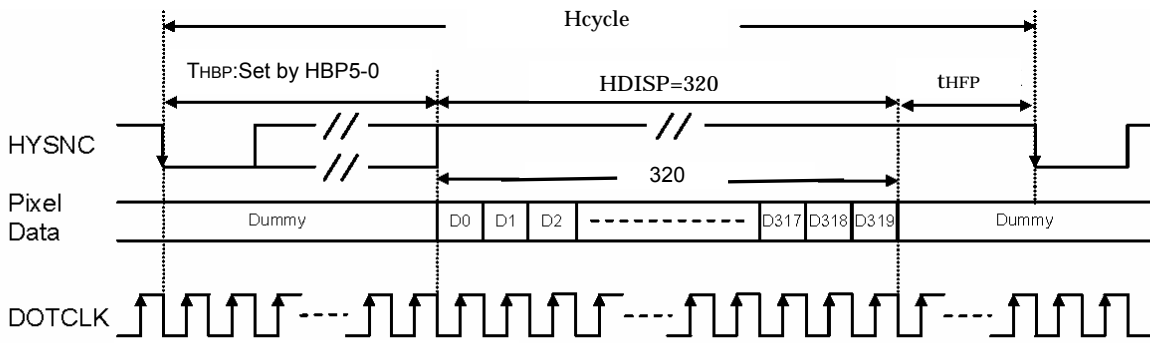
Note 2)

Horizontal Porch(R16h)(POR=9F86h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|-----|-----|-----|------|------|------|------|------|------|
| W | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 |
| POR | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

HBP5-0: Set the delay period from falling edge of HSYNC to first valid line.

| HBP5 | HBP4 | HBP3 | HBP2 | HBP1 | HBP0 | No. of clock cycle of DOTCLK |
|------|------|------|------|------|------|------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 3 |
| 0 | 0 | 0 | 0 | 1 | 0 | 4 |
| 0 | 0 | 0 | 0 | 1 | 1 | 5 |
| 0 | 0 | 0 | 1 | 0 | 0 | 6 |
| ⋮ | | | | | | ⋮ |
| ⋮ | | | | | | Step = 1 |
| ⋮ | | | | | | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 0 | 64 |
| 1 | 1 | 1 | 1 | 1 | 1 | 65 |



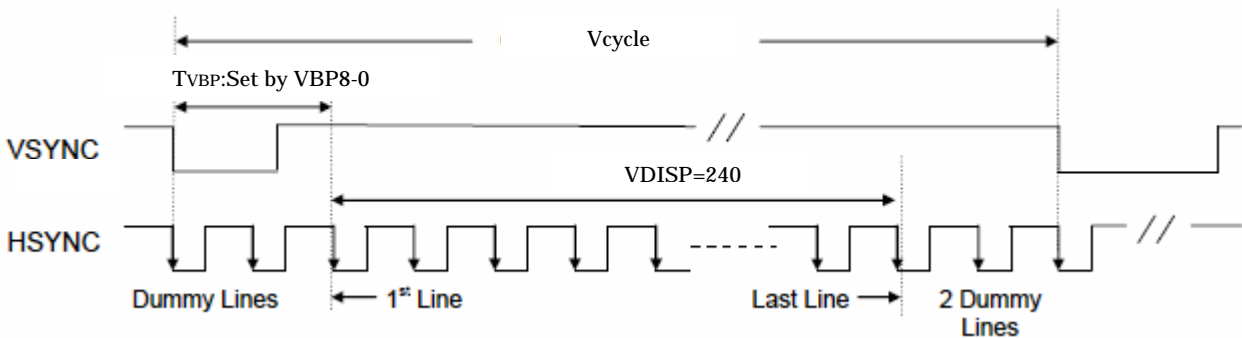
Note 3)

Vertical Porch(R17h)(POR=0002h)

| R/W | DC | IB15 | IB14 | IB13 | IB12 | IB11 | IB10 | IB9 | IB8 | IB7 | IB6 | IB5 | IB4 | IB3 | IB2 | IB1 | IB0 |
|-----|----|------|------|------|------|------|------|-----|------|------|------|------|------|------|------|------|------|
| W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VBP8 | VBP7 | VBP6 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 |
| POR | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

VBP8-0 : Set the delay period from falling edge of VSYNC to first valid line.

| VBP8 | VBP7 | VBP6 | VBP5 | VBP4 | VBP3 | VBP2 | VBP1 | VBP0 | No. of clock cycle of HSYNC |
|------|------|------|------|------|------|------|------|------|------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 (only allow when CAD=0) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| ⋮ | | | | | | | | | ⋮ |
| ⋮ | | | | | | | | | Step = 1 |
| ⋮ | | | | | | | | | ⋮ |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 319 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 320 |
| 1 | 0 | 1 | * | * | * | * | * | * | Reserved |
| 1 | 1 | * | * | * | * | * | * | * | Reserved |



6-3. Back light driving

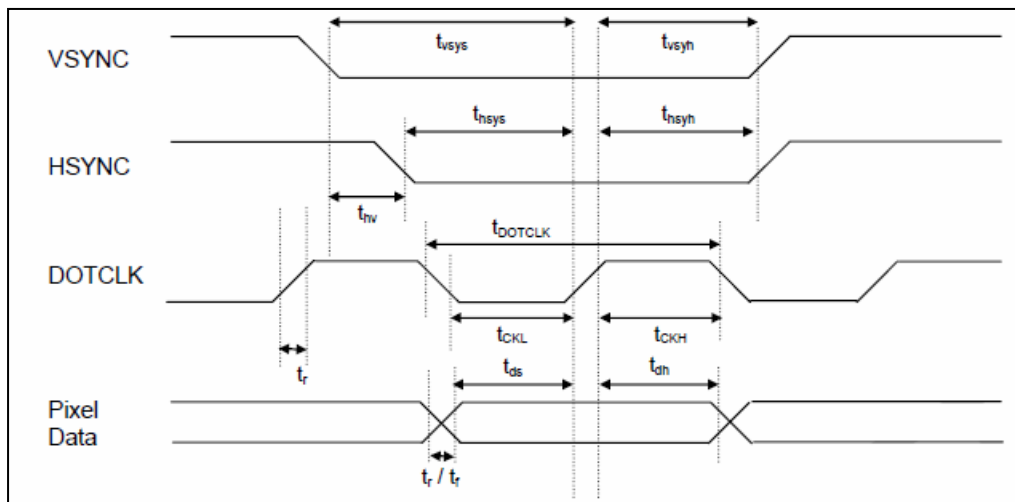
The back light system has 4 LEDs

Used LED : GM4BW64310A[SHARP]

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-------------------|----------|------|------|------|------|---------|
| Rated Voltage | V_{BL} | - | 12.8 | 14.0 | V | |
| Rated Current | I_L | - | 20 | - | mA | Ta=25°C |
| Power consumption | W_L | - | 256 | - | mW | |

7. Timing characteristics of input signals

7-1. Pixel Clock Timing

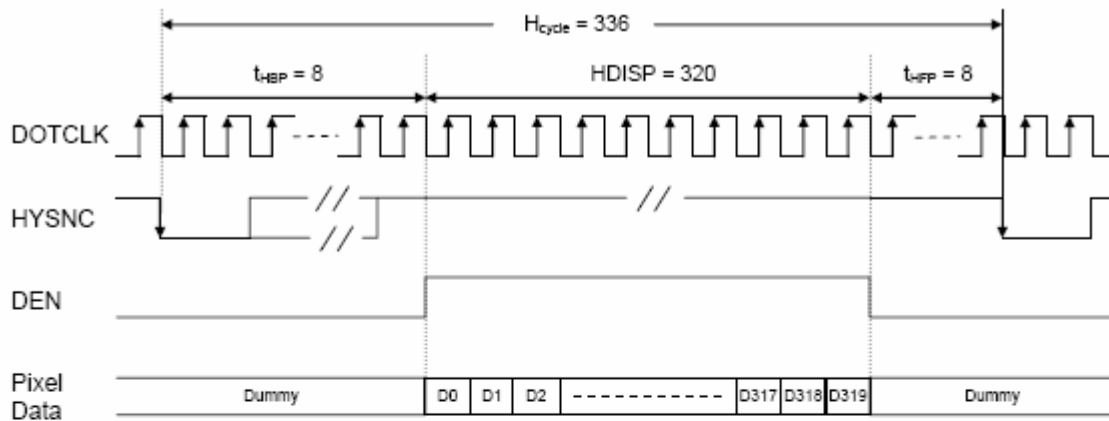


| Characteristics | | Symbol | Min | Typ | Max | Unit |
|--|-------------|--------------|-----|-----|-----|--------------|
| DOTCLK | Frequency | f_{DOTCLK} | - | 5.0 | 8.0 | MHz |
| | Period | t_{DOTCLK} | 125 | 200 | - | nSec |
| | High Period | t_{CKH} | 62 | - | - | nSec |
| | Low Period | t_{CKL} | 62 | - | - | nSec |
| Data | Setup Time | t_{ds} | 30 | - | - | nSec |
| | Hold Time | t_{dh} | 30 | - | - | nSec |
| Vsync | Setup Time | t_{vsys} | 20 | - | - | nSec |
| | Hold Time | t_{vsyh} | 20 | - | - | nSec |
| Hsync | Setup Time | t_{hsys} | 20 | - | - | nSec |
| | Hold Time | t_{hsyh} | 20 | - | - | nSec |
| Phase difference of Sync signal Falling edge | | t_{hv} | 0 | - | 320 | t_{DOTCLK} |
| Reset Pulse Width | | t_{RES} | 10 | - | - | nSec |
| Rise / Fall Time | | t_r/t_f | 20 | - | 100 | nSec |

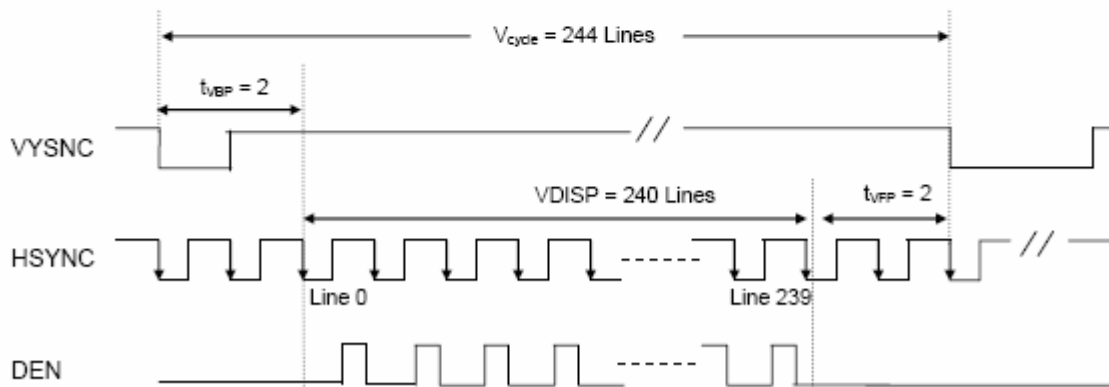
Note: External clock source must be provided to DOTCLK pin.

The module will not operate if absent of the clocking signal.

7-2. Data Transaction Timing in Normal Operating Mode (262k color)



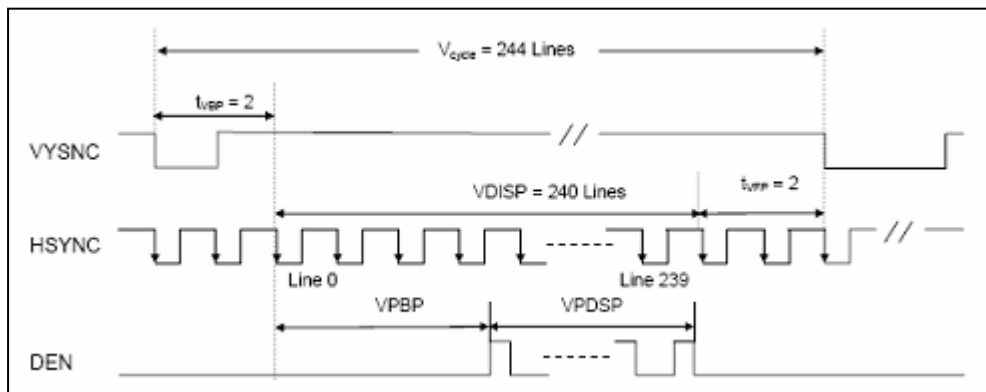
a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

| Characteristics | | Symbol | Min | Typ | Max | Unit |
|-----------------------------|-----------|---------------------------------|-----|------|-------|-------|
| DOTCLK | Frequency | f_{DOTCLK} | - | 5.0 | 8.0 | MHz |
| | Period | t_{DOTCLK} | 125 | 200 | - | ns |
| HSYNC | Frequency | f_h | - | 14.9 | 18.18 | kHz |
| | Cycle | H_{cycle} | - | 336 | - | clock |
| VSYNC | Frequency | f_v | 50 | 60.1 | - | Hz |
| | Cycle | V_{cycle} | - | 244 | - | line |
| Horizontal Back Porch | | t_{HBP} | - | 8 | - | clock |
| Horizontal Front Porch | | t_{HFP} | - | 8 | - | clock |
| Horizontal Data Start Point | | t_{HBP} | - | 8 | - | clock |
| Horizontal Blanking Period | | $t_{\text{HBP}}+t_{\text{HFP}}$ | - | 16 | - | clock |
| Horizontal Display Area | | HDISP | - | 320 | - | clock |
| Vertical Back Porch | | t_{VBP} | - | 2 | - | line |
| Vertical Front Porch | | t_{VFP} | - | 2 | - | line |
| Vertical Data Start Point | | t_{VBP} | - | 2 | - | line |
| Vertical Blanking Period | | $t_{\text{HBP}}+t_{\text{HFP}}$ | - | 4 | - | line |
| Vertical Display Area | | VDISP | - | 240 | - | line |

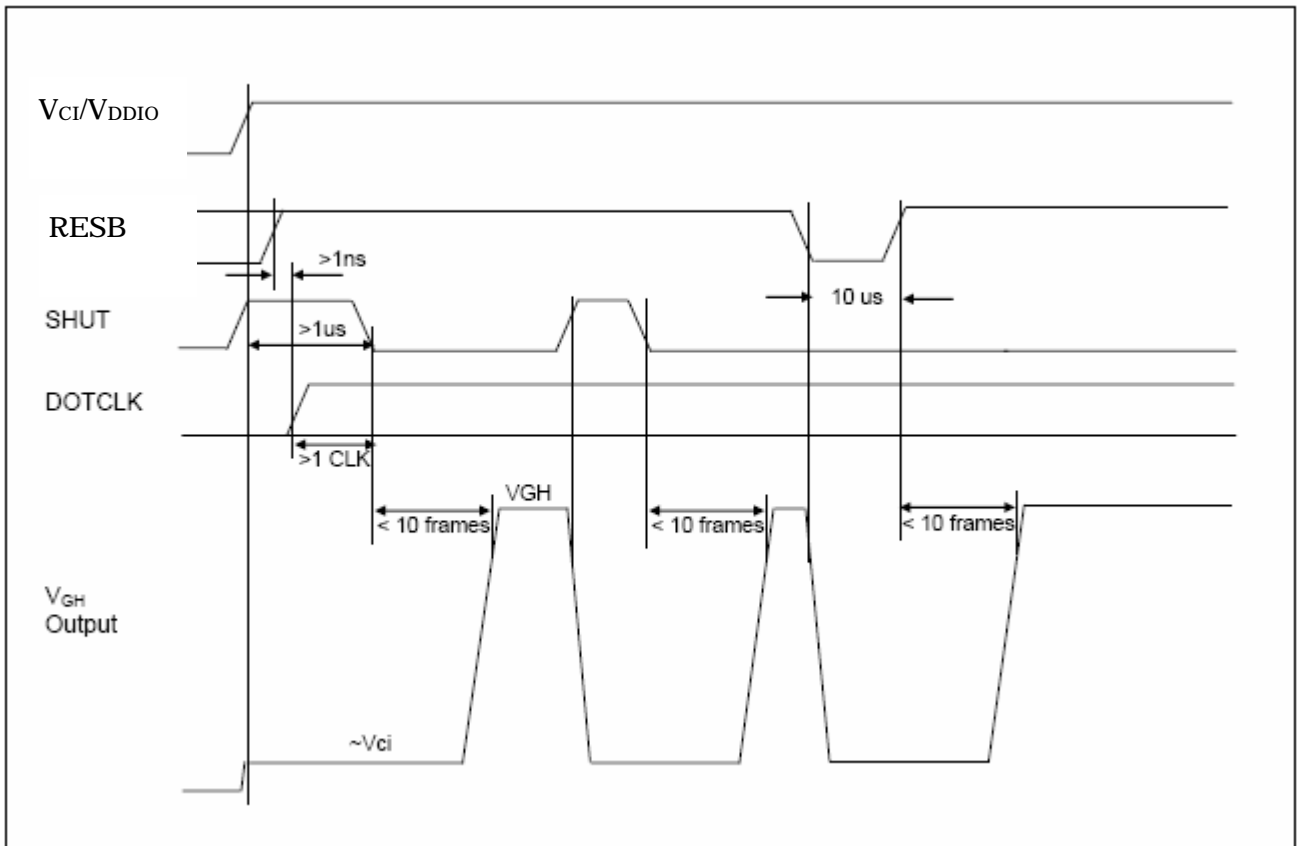
7-3. Synchronization Signals Timing in Power Save Mode (8 color)



| Characteristics | | Symbol | Min | Typ | Max | Unit |
|-----------------------------|-----------|--------------|-----|------|-------|------|
| DOTCLK | Frequency | f_{DOTCLK} | - | 5.0 | 8.0 | MHz |
| | Period | t_{DOTCLK} | 125 | 200 | - | ns |
| HSYNC | Frequency | f_h | - | 14.9 | 18.18 | kHz |
| VSYNC | Frequency | f_v | 50 | 60.1 | - | Hz |
| | Cycle | V_{cycle} | - | 244 | - | line |
| Vertical Partial Back Porch | | VPBP | 0 | - | 239 | line |
| Vertical Active Area | | VPDSP | 1 | - | 240 | line |
| Vertical Back Porch | | t_{VBP} | - | 2 | - | line |
| Vertical Front Porch | | t_{VFP} | - | 2 | - | line |
| Vertical Display Area | | V_DISP | - | 240 | - | line |

Note : When entered to 8-color display mode, the RGB graphic data through the interface pin RR5, GG5 and BB5 are valid within the Vertical Active Area. Data "0" will be displayed the Vertical Active Area.

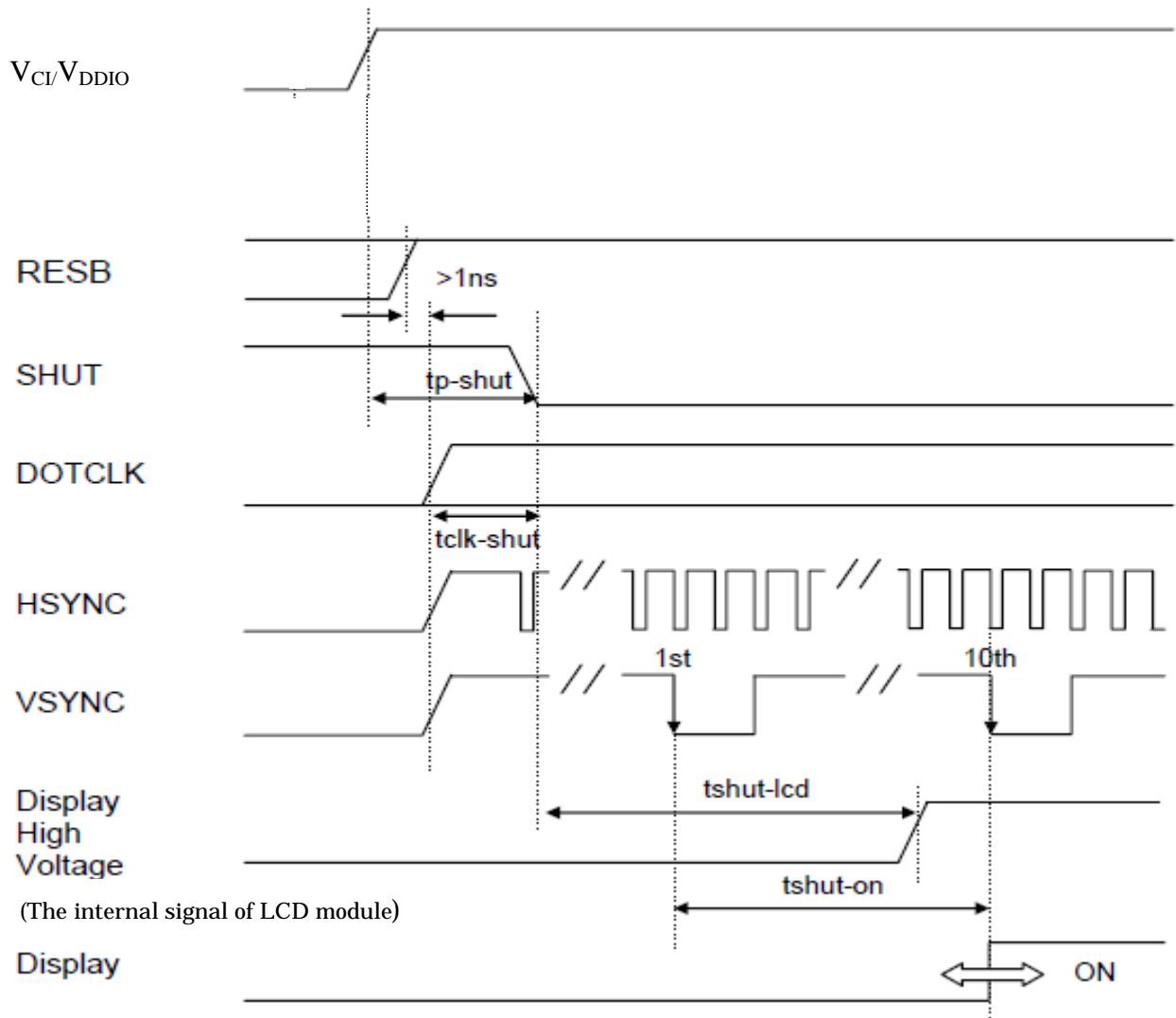
7-4. V_{GH} Output against SHUT & RESB



V_{GH} Output against SHUT & RESB

- Note1:** The minimum cycle time of SHUT is $10 + 2$ frames.
- Note2:** DOTCLK must be provided for boosting of V_{GH} . The above timing diagram assumed voltages and DOTCLK are continuous supplied after power on.
- Note3:** V_{GH} will be forced to V_{ci} at the low stage of | RESB.
- Note4:** The minimum pulse width of RESET is $10\mu s$.

7-5. Power Up Sequence

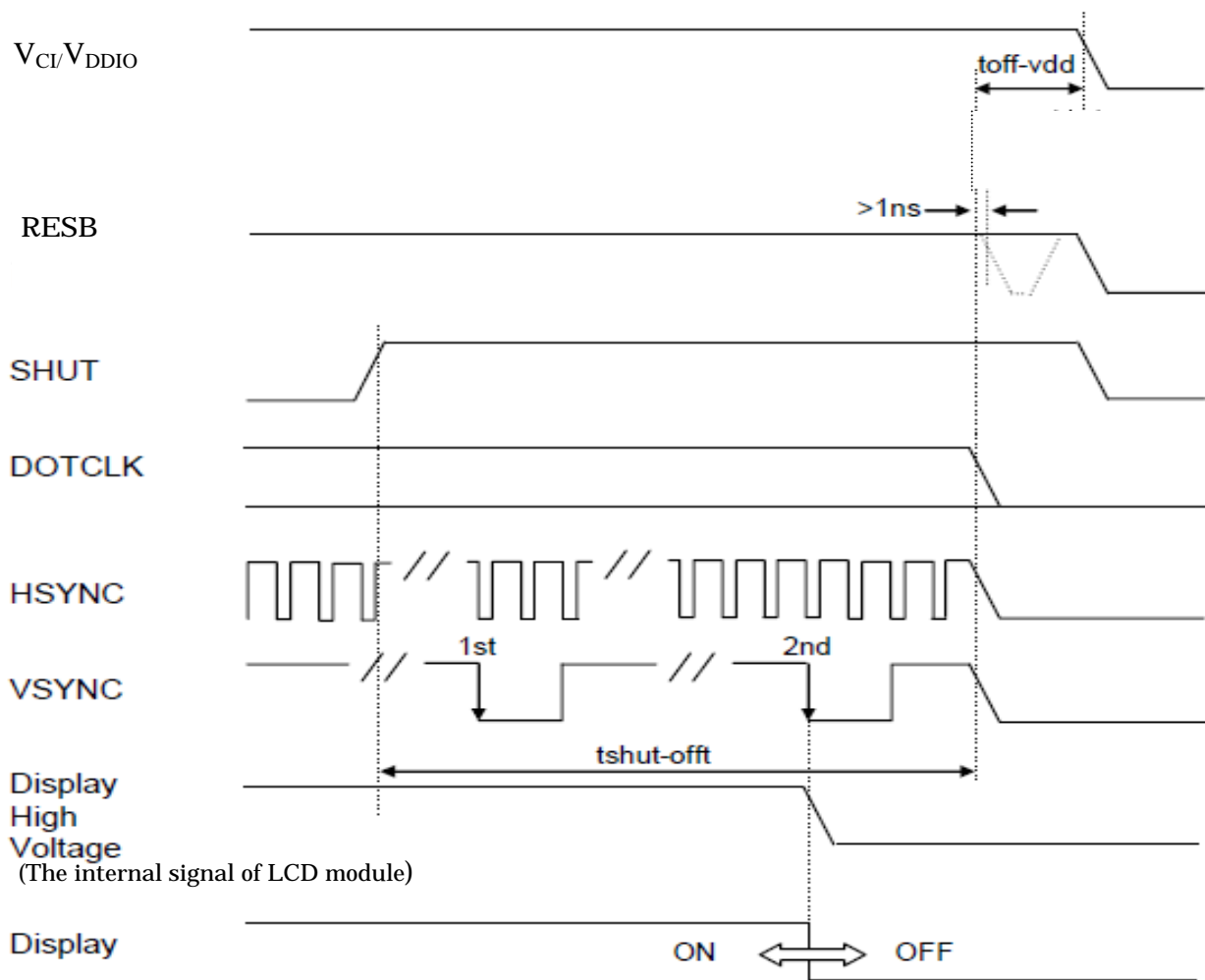


| Characteristics | Symbol | Min | Typ | Max | Units |
|---|-----------|-----|-----|-----|-------|
| V _{DDEXT} / V _{DDIO} on to falling edge of SHUT | tp-shut | 1 | - | - | μsec |
| DOTCLK | tclk-shut | 1 | - | - | clk |
| Falling edge of SHUT to LCD power on | tshut-lcd | - | - | 164 | msec |
| Falling edge of SHUT to display start | tshut-on | - | - | 10 | frame |
| -- 1 line: 336 clk | | - | 164 | - | msec |
| -- 1 frame: 244 line | | - | - | - | - |
| -- DOTCLK = 5.0MHz | | | | | |

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSYNC after the falling edge of SHUT.

7-6. Power Down Sequence



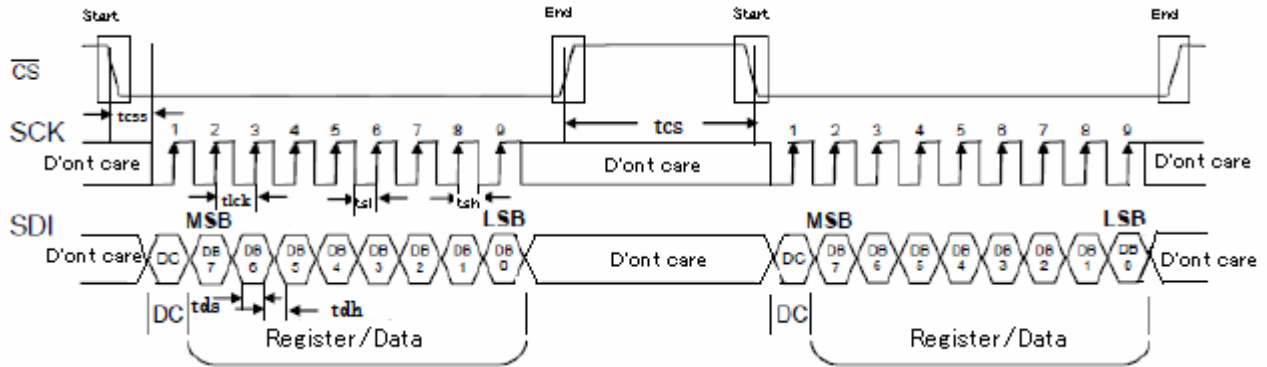
| Characteristics | Symbol | Min | Typ | Max | Units |
|---|-----------|------|-----|-----|-------|
| Rising edge of SHUT to display off | tshut-off | 2 | - | - | frame |
| -- 1 line: 336 clk -- 1 frame: 244 line -- DOTCLK = 5.0 MHz | | 32.8 | - | - | msec |
| Input-signal-off to V _{DDEXT} / V _{DDIO} off | toff-vdd | 1 | - | - | μsec |

Note1: DOTCLK must be maintained at least 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling of VSYNC after the falling edge of SHUT.

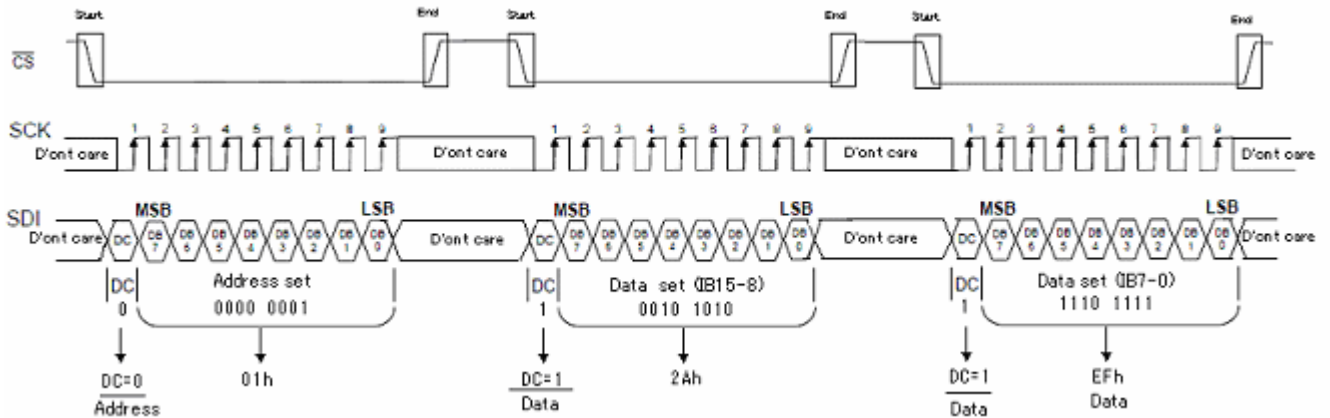
Note3: IF RESET(RES) signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

7-7. SPI Interface Timing Diagram & Transaction Example (9 bit)

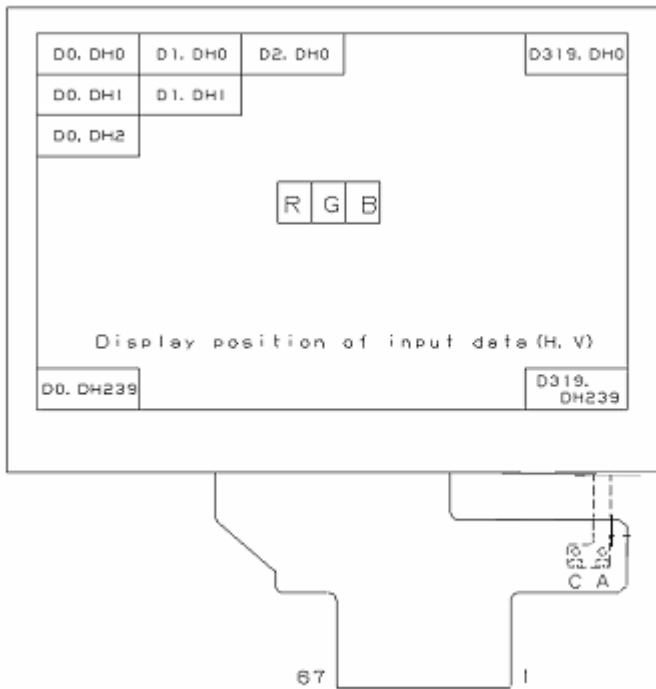


| Characteristics | | 記号 | Min | Typ | Max | 単位 |
|-----------------|-----------------|------|-----|-----|-----|-----|
| Serial Clock | Frequency | fclk | - | - | 20 | MHz |
| | Cycle Time | tclk | 50 | - | - | ns |
| | Low Width | tsl | 25 | - | - | ns |
| | High Width | tsh | 25 | - | - | ns |
| Chip Select | Setup Time | tcss | 0 | - | - | ns |
| | Hold time | tcsh | 10 | - | - | ns |
| | High Delay Time | tcsd | 20 | - | - | ns |
| Data | Setup Time | tds | 5 | - | - | ns |
| | Hold Time | tdh | 10 | - | - | ns |

The example transmit "0x2AEFh" to register R01h.



7-8. Input Data Signals and Display Position on the screen



Please refer to Input Terminal Names and Functions

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

| | Colors & | Date signal | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----------|-------------|-----|----|----|----|----|----|-----|----|----|----|----|----|-----|----|----|----|----|----|-----|--|--|--|
| | | Gray | R0 | R1 | R2 | R3 | R4 | R5 | G0 | G1 | G2 | G3 | G4 | G5 | B0 | B1 | B2 | B3 | B4 | B5 | | | | |
| | | Scale | LSB | | | | | | MSB | | | | | | LSB | | | | | | MSB | | | |
| Basic Color | Black | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Blue | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |
| | Green | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Cyan | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |
| | Red | - | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Magenta | - | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |
| | Yellow | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | White | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |
| Gray Scale of Red | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | GS1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Darker | GS2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | ↓ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | Brighter | GS61 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↓ | GS62 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Red | GS63 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| Gray Scale of Green | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | GS1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Darker | GS2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | ↓ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | Brighter | GS61 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↓ | GS62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Green | GS63 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| Gray Scale of Blue | Black | GS0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | GS1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | | | | |
| | Darker | GS2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | | |
| | ↑ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | ↓ | ↓ | ↓ | | | | | | ↓ | | | | | | ↓ | | | | | | | | | |
| | Brighter | GS61 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | | | | |
| | ↓ | GS62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | | | | |
| | Blue | GS63 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | |

0: Low level voltage, 1: High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals.
According to the combination of 18 bit data signals, the 262k color display can be achieved on the screen.

9. Optical Characteristics

Ta = 25°C, V_{DDIO} = +3.3V, V_{CI} = +3.3V

| Parameter | | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark | |
|---------------------------------|------------|-----------------|-----------------------|------|------|------|------|-------------------|------------------------|
| Viewing angle range (Wide View) | Horizontal | θ21 | CR 10 | - | 80 | - | deg. | 【Note1,4】 | |
| | | θ22 | | - | 80 | - | deg. | | |
| | Vertical | θ11 | | - | 80 | - | deg. | | |
| | | θ12 | | - | 80 | - | deg. | | |
| Contrast ratio | | CR | Optimum viewing angle | 300 | 500 | - | | 【Note2,4】 | |
| Response Time | Rise | τ _r | θ=0° | - | 15 | 30 | ms | 【Note3,4】 | |
| | Decay | τ _d | | - | 15 | 30 | ms | | |
| Chromaticity of White | | x | | 0.26 | 0.31 | 0.36 | - | 【Note4】 | |
| | | y | | 0.29 | 0.34 | 0.39 | - | | |
| Luminance of white | | X _{L1} | | | 250 | 350 | - | cd/m ² | I _{LED} =20mA |

* The optical characteristics measurements are operated under a stable luminescence (I_{LED} = 20mA) and a dark condition. (Refer to Fig.9-1)

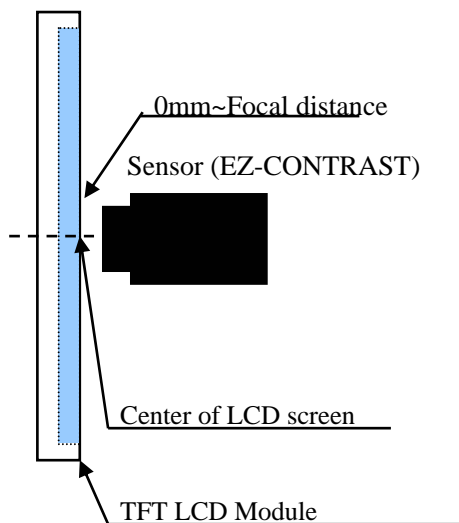


Fig.9-1 Measuring setup for Viewing angle and Contrast ratio (BM-7 is used for contrast.)

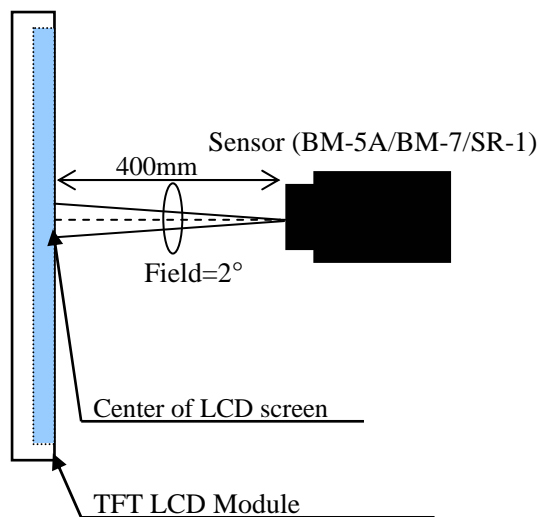
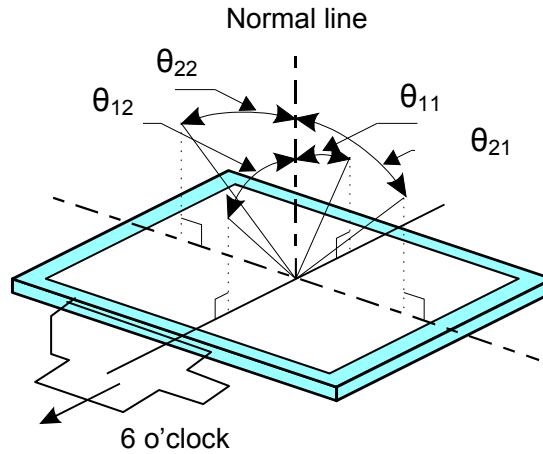


Fig.9-2 Measuring setup for Luminance, Chromaticity and Response time (BM-7 is used for Luminance, SR-1 is for response)

【 Note 1 】 Definitions of viewing angle range



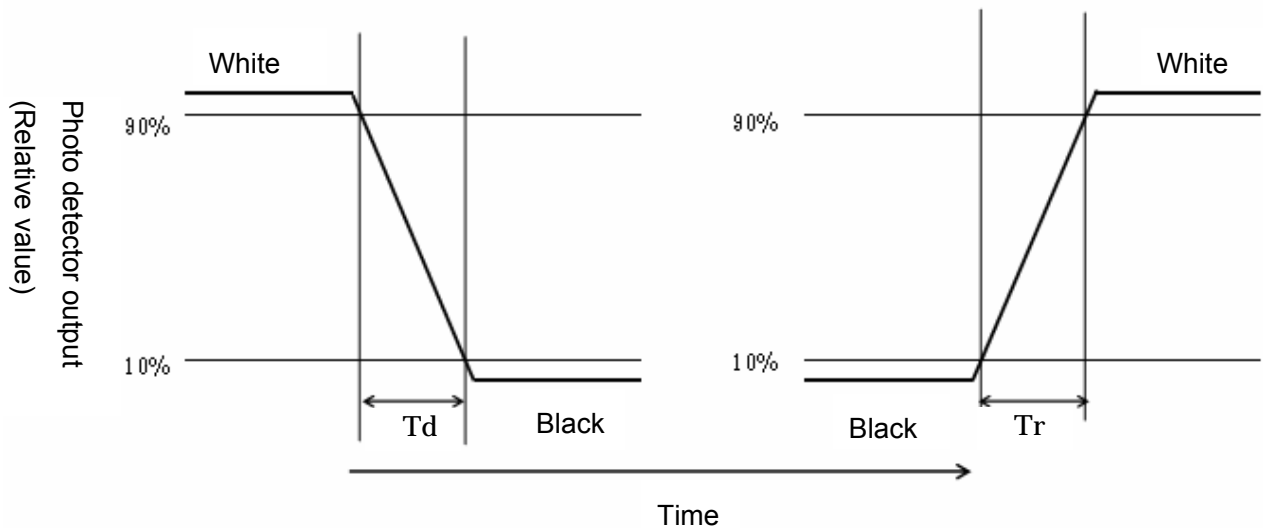
【 Note 2 】 Definition of contrast ratio

The contrast ratio is defined as the following

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

【 Note 3 】 Definition of response time

The response time is defined as the following figure and shall be measured by switching the input signal for “Black” and “White”



【 Note 4 】 This shall be measured at center of the screen.

10 Handling of modules

10-1. Inserting the FPC into its connector and pulling it out

- 1) Be sure to turn off the power supply and the signals when inserting or disconnecting the cable.
- 2) Please insert for too much stress not to join FPC in the case of insertion of FPC.

10-2. About handling of FPC

- 1) The bending radius of the FPC should be more than 1.4mm, and it should be bent evenly.
- 2) Do not dangle the LCD module by holding the FPC, or do not give any stress to it.

10-3. Mounting of the module

- 1) The module should be held on to the plain surface. Do not give any warping or twisting stress to the module.
- 2) Please consider that GND can ground a modular metal portion etc. so that static electricity is not charged to a module.

10-4. Cautions in assembly / Handling pre cautions

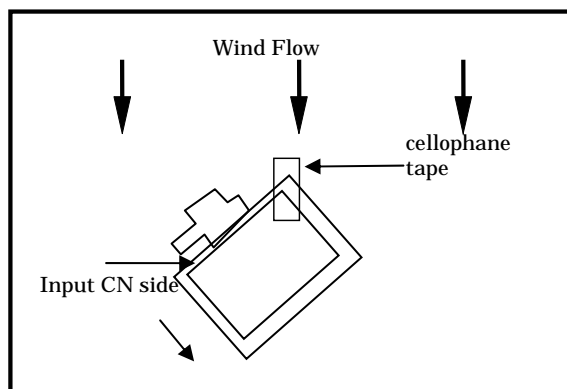
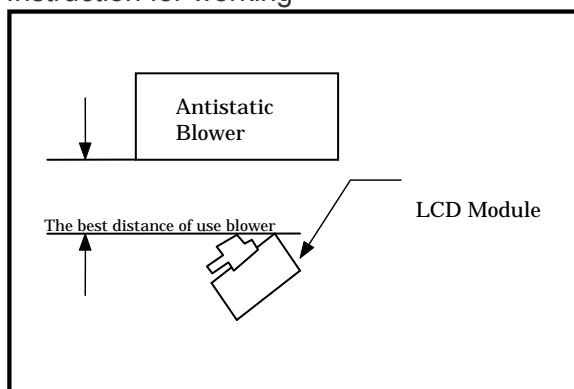
As the polarizer can be easily scratched, be most careful in handling it.

1) Work environments in assembly.

Since removing laminator may causes electrostatic charge that tends to attract dust, the following work environment would be desired.

- a) Floor: Conductive treatment having 1MΩ resistance onto floor's tile
- b) The room free from dust coming from outdoor environment, and put an adhesive mat at entrances.
- c) Humidity from 50% to 70% and temperature from 15°C to 27°C are desirable.
- d) Worker should ware conductive shoes, conductive fatigue, conductive glove and earth wrist band.

2) Instruction for working



- a) Wind direction of an antistatic blower should slightly downward to properly blow the module. The distance between the blower and the module should be the best distance of use blower. Also, pay attention to the direction of the module.
- b) To prevent polarizer from scratching, adhesive tape (cellophane tape) should be stuck at the part of laminator sheet, which is closed to blower. [See the above]
- c) Pull slowly adhesive tape to peel the laminator off, with spending more than 5 second.
- d) The module without laminator should be moved to the next process to prevent adhesion of dust.

- 3) How to remove dust on the polarizer
 - a) Blow out dust by the use of an N2 blower with antistatic measures taken. Use of an ionized air Gun is recommendable.
 - b) When the panel surface is soiled, wipe it with soft cloth.
- 4) In the case of the module's metal part (shield case) is stained, wipe it with a piece of dry, soft cloth. If rather difficult, give a breath on the metal part to clean better.
- 5) If water dropped, etc. remains stuck on the polarizer for a long time, it is apt to get discolored or cause stains. Wipe it immediately.
- 6) As a glass substrate is used for the TFT-LCD panel, if it is dropped on the floor or hit by something hard, it may be broken or chipped off.
- 7) Since CMOS LSI is used in this module, take care of static electricity and take the human earth into consideration when handling.

10-5. Others

- 1) Regarding storage of LCD modules, avoid storing them at direct sunlight-situation.
- 2) If stored at temperatures below the rated values, the inner liquid crystal may freeze, causing cell destruction. At temperatures exceeding the rated values for storage, the liquid crystal may become isotropic liquid, making it no longer possible to come back to its original state in some cases.
- 3) If the LCD is broken, do not drink liquid crystal in the mouth. If the liquid crystal adheres to a hand or foot or to clothes, immediately cleanse it with soap.
- 4) If a water drop or dust adheres to the polarizer, it is apt to cause deterioration. Wipe it immediately.
- 5) Be sure to observe other caution items for ordinary electronic parts and components.

11. Reliability test items

| No. | Test item | Conditions |
|-----|---|--|
| 1 | High temperature storage test | Leaves the module at Ta=+70°C for 240h |
| 2 | Low temperature storage test | Leaves the module at Ta=-25°C for 240h |
| 3 | High temperature & high humidity operation test | Operates the module at Ta=+40°C; 95%RH for 240h (No condensation) |
| 4 | High temperature operation test | Operates the module with +60°C at panel surface for 240h |
| 5 | Low temperature operation test | Operates the module at Ta=-10°C for 240h |
| 6 | Vibration test (non- operating) | Frequency range: 10 to 55Hz Stroke: 1.5mm Sweep time: 1minutes Test period: 2 hours for each direction of X,Y,Z |
| 7 | Shock test | Direction: ±X, ±Y, ±Z, Time: Third for each direction. Impact value: 980m/s ² , Action time 6ms |
| 8 | Thermal shock test | Ta=-10°C to 70°C /10 cycles (30 min) (30min) |

【Note】 Ta = Ambient temperature, Tp = Panel temperature

【Check items】

In the standard condition, there shall be no practical problems that may affect the display function.

12. Display Grade

The standard regarding the grade of color LCD displaying modules should be based on the delivery inspection standard.

13. Delivery Form

1) Carton piling-up: Max 8 rows

2) Environments

Temperature: 0 ~ 40°C

Humidity: 65% RH or less (at 40°C)

There should be no dew condensation even at a low temperature and high humidity.

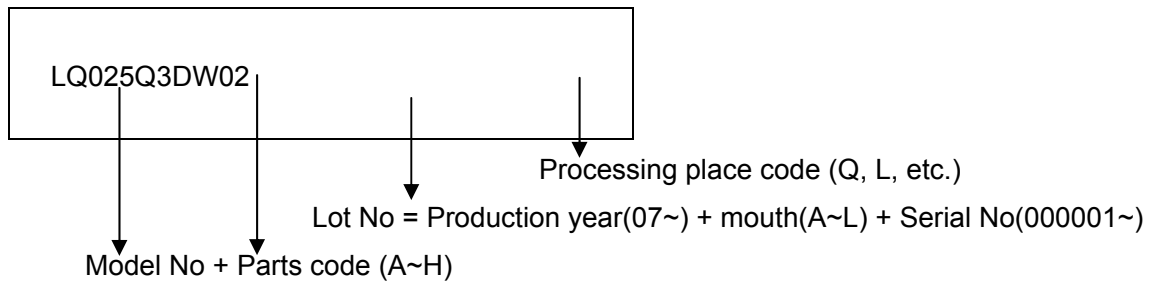
3) Packing form: 15. LCD module packing carton

Cartons are weak against damp, and they are apt to be smashed easily due to the compressive pressure applied when piled up. The above environmental conditions of temperature and humidity are set in consideration of reasonable pile-up for storage.

14. Lot No. marking

The lot No. will be indicated on individual labels. The location is as shown

Indication Label

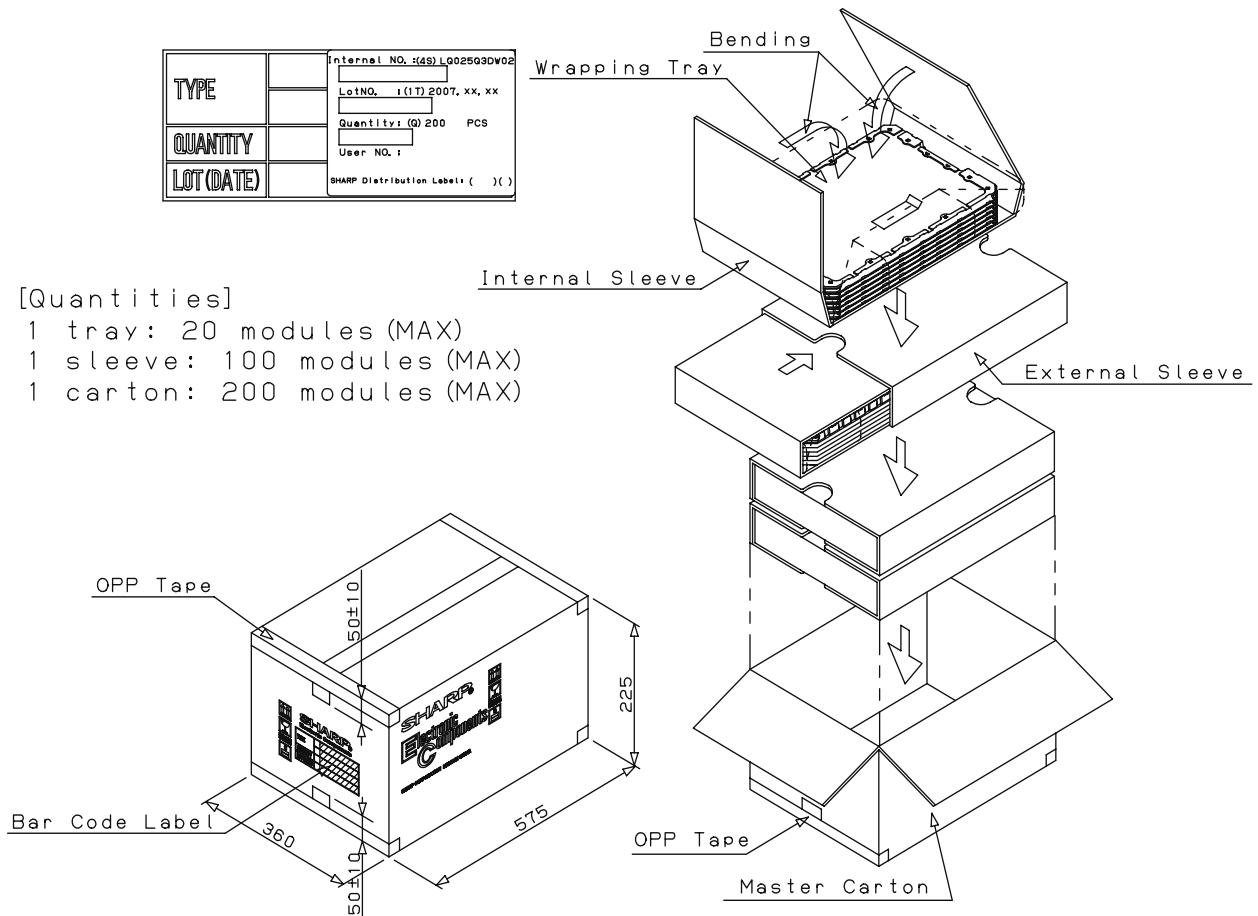


15. LCD module packing carton

| | | |
|------------|--|-----------------------------------|
| TYPE | | Internal NO. (4S) LQ025Q3DW02 |
| QUANTITY | | LotNO. i(1T)2007, xx, xx |
| LOT (DATE) | | Quantity: (Q) 200 PCS |
| | | User NO. : |
| | | SHARP Distribution Label: () () |

[Quantities]

- 1 tray: 20 modules (MAX)
- 1 sleeve: 100 modules (MAX)
- 1 carton: 200 modules (MAX)

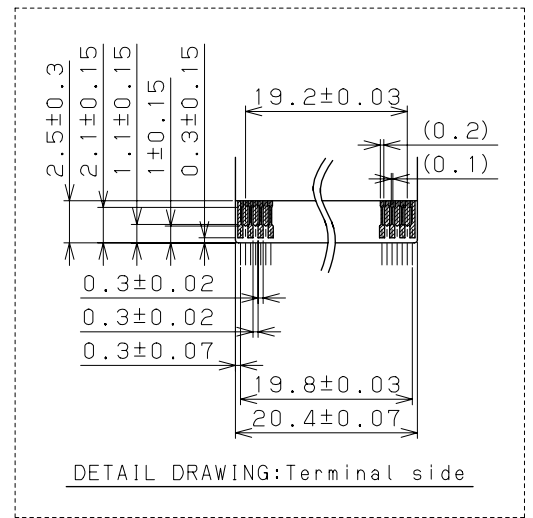
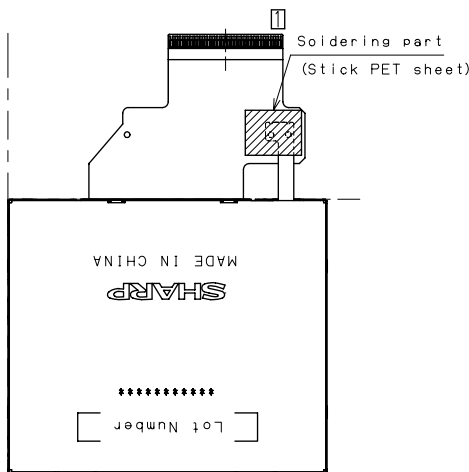
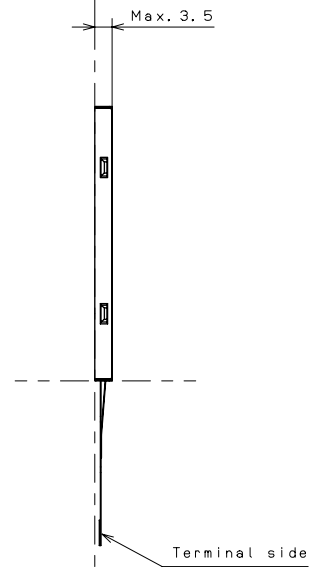
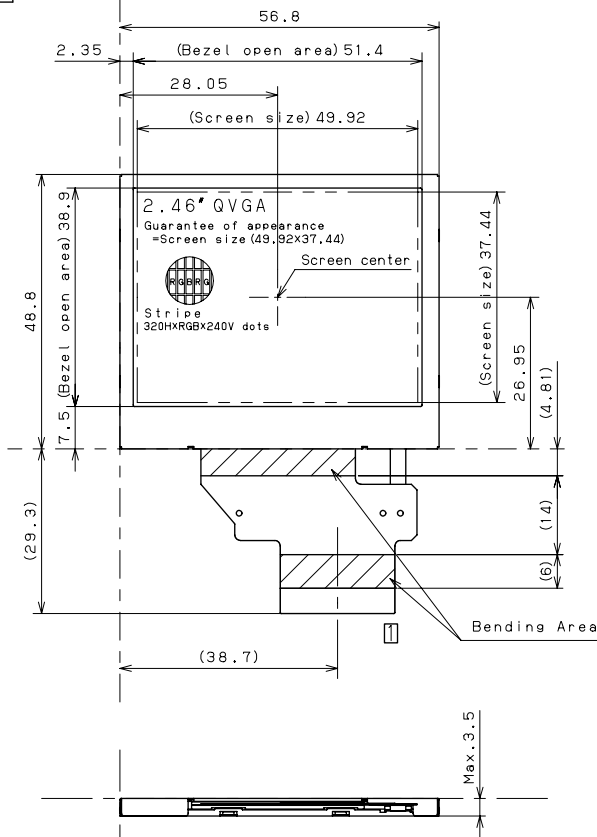


16. Others

- 1 Disassembling the module can cause permanent damage and you should be strictly avoided.
- 2 Please be careful that you don't keep the screen displayed fixed pattern image for a long time, since retention may occur.
- 3 If you pressed down a liquid crystal display screen with your finger and so on, the alignment disorder of liquid crystal will occur. And then It will become display fault.
Therefore, be careful not to touch the screen directly, and to consider not stressing to it.
- 4 If any problem arises regarding the items mentioned in this specification sheet or otherwise, it should be discussed and settled mutually in a good faith for remedy and/or improvement.

SHARP

Outline proposal



Recommended connector: FH26G (HIROSE ELECTRIC CO., LTD.) or 6281 (KYOCERA ELCO CORP.)

- 1) General tolerance is ± 0.5 .
- 2) Guarantee of appearance = LCD Active Area.
- 3) Tolerance of thickness does not include any wrinkling of PET tape or any loose PET tape off the FPC.
- 4) LCD-FPC should be bent only in the bending area.
- 5) LCD/LED FPC bend larger than 0.6 in radius.
- 6) Take care in set design to hide the scratches and bubbles appeared on the polarizer or other frame area which is located outside of the guarantee area.
- 7) The light of Back Light is leaking from the BM outside, please use light shielding in the set.
- 8) The tolerance of the module width area excludes warp of the case.

Since this module is under development, all the specified values are tentative. The technical literature is subject to change without notice.

| | | | | | |
|------------|---|-------|---------------|-------------------------------------|--------------------------------|
| unit:mm | Please do not copy this material and do not disclose this to a third party. | | | | |
| DATE | 2007. 10. 01 | SCALE | free | | |
| MODEL | L'Q'0'2'5'Q'3'D'W'0'2' | | | | |
| DRAWING NO | L'CM'1'1'-0'7'3'7'A | size | A3 | DATE | REVISION |
| | | | | | |
| | | | SHARP CO. LTD | ENGINEERING DEPARTMENT | MOBILE LIQUID CRYSTAL DIVISION |
| | | | | MOBILE LIQUID CRYSTAL DISPLAY GROUP | Sign. |

LCD Specification

LCD Group



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