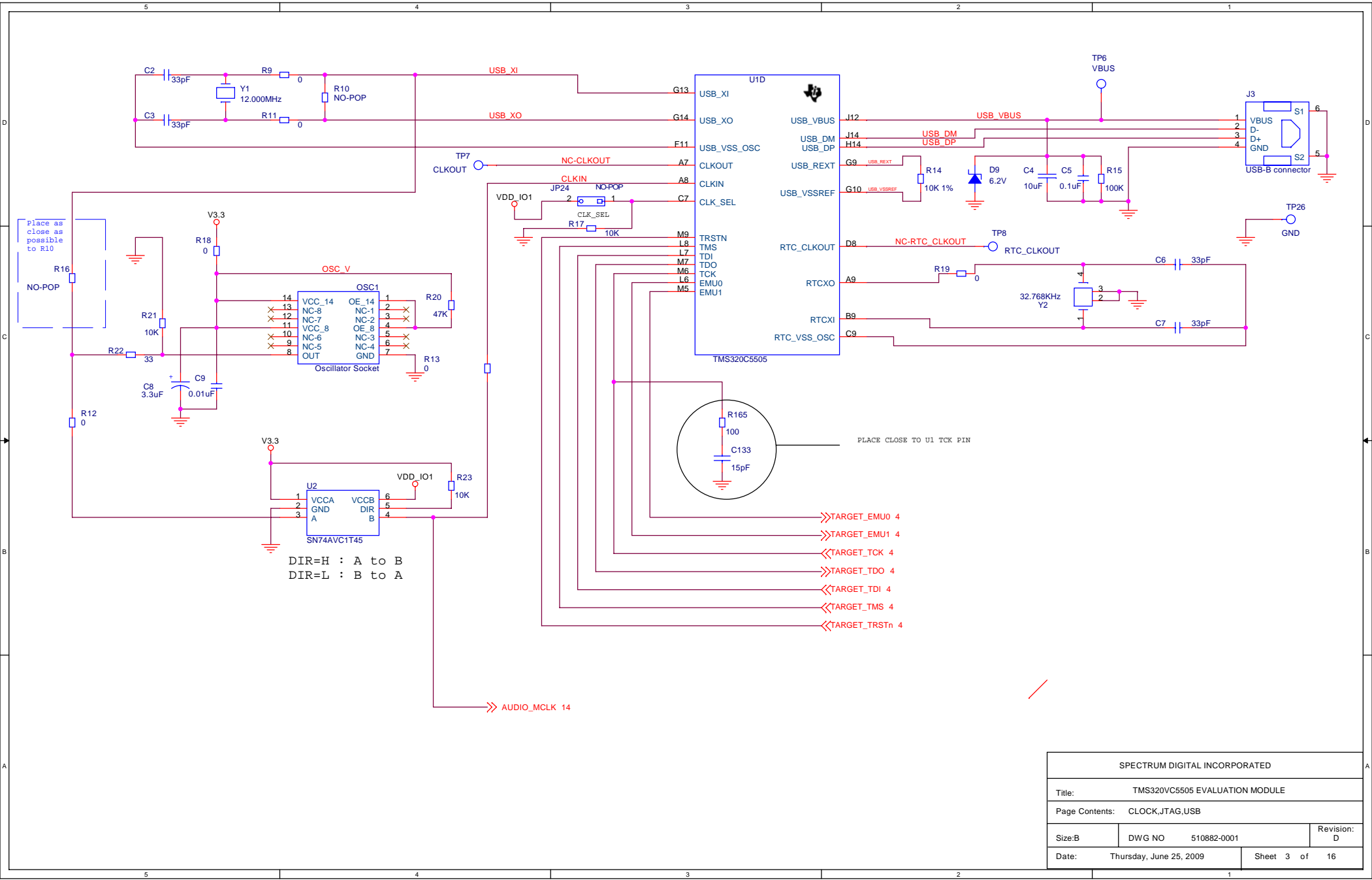


Pin	Signal	External Component	Internal Signal
L10	GPIO0	MMC0_CLK 11,13	GPIO0 I2S0_CLK 11,13
M11	GPIO1	MMC0_CMD 11,13	GPIO1 I2S0_FS 11,13
L9	GPIO2	MMC0_DATA0 11,13	GPIO2 I2S0_DX 11,13
M10	GPIO3	MMC0_DATA1 11,13	GPIO3 I2S0_RX 11,13
L12	GPIO4	MMC0_DATA2 11,13	GPIO4 GPIO4 11,13
L11	GPIO5	MMC0_DATA3 11,13	GPIO5 GPIO5 11,13
M13	GPIO6	MMC1_CLK 13	GPIO6 I2S1_CLK 13
L14	GPIO7	MMC1_CMD 13	GPIO7 I2S1_FS 13
M14	GPIO8	MMC1_DATA0 13	GPIO8 I2S1_DX 13
M12	GPIO9	MMC1_DATA1 13	GPIO9 I2S1_RX 13
K14	GPIO10	MMC1_DATA2 13,14	GPIO10 GPIO10 13,14
L13	GPIO11	MMC1_DATA3 8,13	GPIO11 GPIO11 8,13
P6	LCD_DATA0	LCD_DATA[0:15] 6,12,13,14,15	LCD_DATA[0:15] 6,12,13,14,15
N6	LCD_DATA1		
P7	LCD_DATA2		
N7	LCD_DATA3		
N8	LCD_DATA4		
N9	LCD_DATA5		
P10	LCD_DATA7		
N10	LCD_DATA8	LCD_DATA8	I2S2_CLK 6,12,13,14
P11	LCD_DATA9	LCD_DATA9	I2S2_FS 6,12,13,14
N11	LCD_DATA10	LCD_DATA10	I2S2_RX 6,12,13,14
P12	LCD_DATA11	LCD_DATA11	I2S2_DX 6,12,13,14
N12	LCD_DATA12	LCD_DATA12	I2S3_CLK 6,12
P13	LCD_DATA13	LCD_DATA13	I2S3_FS 6,12
N13	LCD_DATA14	LCD_DATA14	I2S3_RX 6,12
P14	LCD_DATA15	LCD_DATA15	I2S3_DX 6,12
N3	LCD_RE	LCD_RE	LCD_RE 6,15
P4	LCD_BIAS_OE	LCD_BIAS_OE	LCD_BIAS_OE 6,15
N4	LCD_MCLK	LCD_MCLK	LCD_MCLK
P5	LCD_nWE	LCD_nWE	LCD_nWE 6,15
N5	LCD_ALE	LCD_ALE	LCD_ALE 6,15
I2S2_CLK	LCD_DATA8	SPI_CLK 6,12,13,14	SPI_CLK 6,12,13,14
I2S2_FS	LCD_DATA9	SPI_CS0 6,12,13,14	SPI_CS0 6,12,13,14
I2S2_RX	LCD_DATA10	SPI_RX 6,12,13,14	SPI_RX 6,12,13,14
I2S2_DX	LCD_DATA11	SPI_DX 6,12,13,14	SPI_DX 6,12,13,14
LCD_BIAS_OE	LCD_BIAS_OE	SPI_ALT_CS0 6,15	SPI_ALT_CS0 6,15
LCD_MCLK	LCD_MCLK	SPI_ALT_CS1 6	SPI_ALT_CS1 6
LCD_nWE	LCD_nWE	SPI_ALT_CS2 6,15	SPI_ALT_CS2 6,15
LCD_ALE	LCD_ALE	SPI_ALT_CS3 6,15	SPI_ALT_CS3 6,15
LCD_RE	LCD_RE	SPI_ALT_CLK 6,15	SPI_ALT_CLK 6,15
LCD_DATA0	LCD_DATA0	SPI_ALT_RX 6,15	SPI_ALT_RX 6,15
LCD_DATA1	LCD_DATA1	SPI_ALT_DX 6,15	SPI_ALT_DX 6,15
LCD_DATA2	LCD_DATA2	GPIO12 6,15	GPIO12 6,15
LCD_DATA3	LCD_DATA3	GPIO13 6,15	GPIO13 6,15
LCD_DATA4	LCD_DATA4	GPIO14 6,15	GPIO14 6,15
LCD_DATA5	LCD_DATA5	GPIO15 6,15	GPIO15 6,15
LCD_DATA6	LCD_DATA6	GPIO16 6,15	GPIO16 6,15
LCD_DATA7	LCD_DATA7	GPIO17 6,15	GPIO17 6,15

SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: GPIO,MMC-SD,SPI,I2C,I2S			
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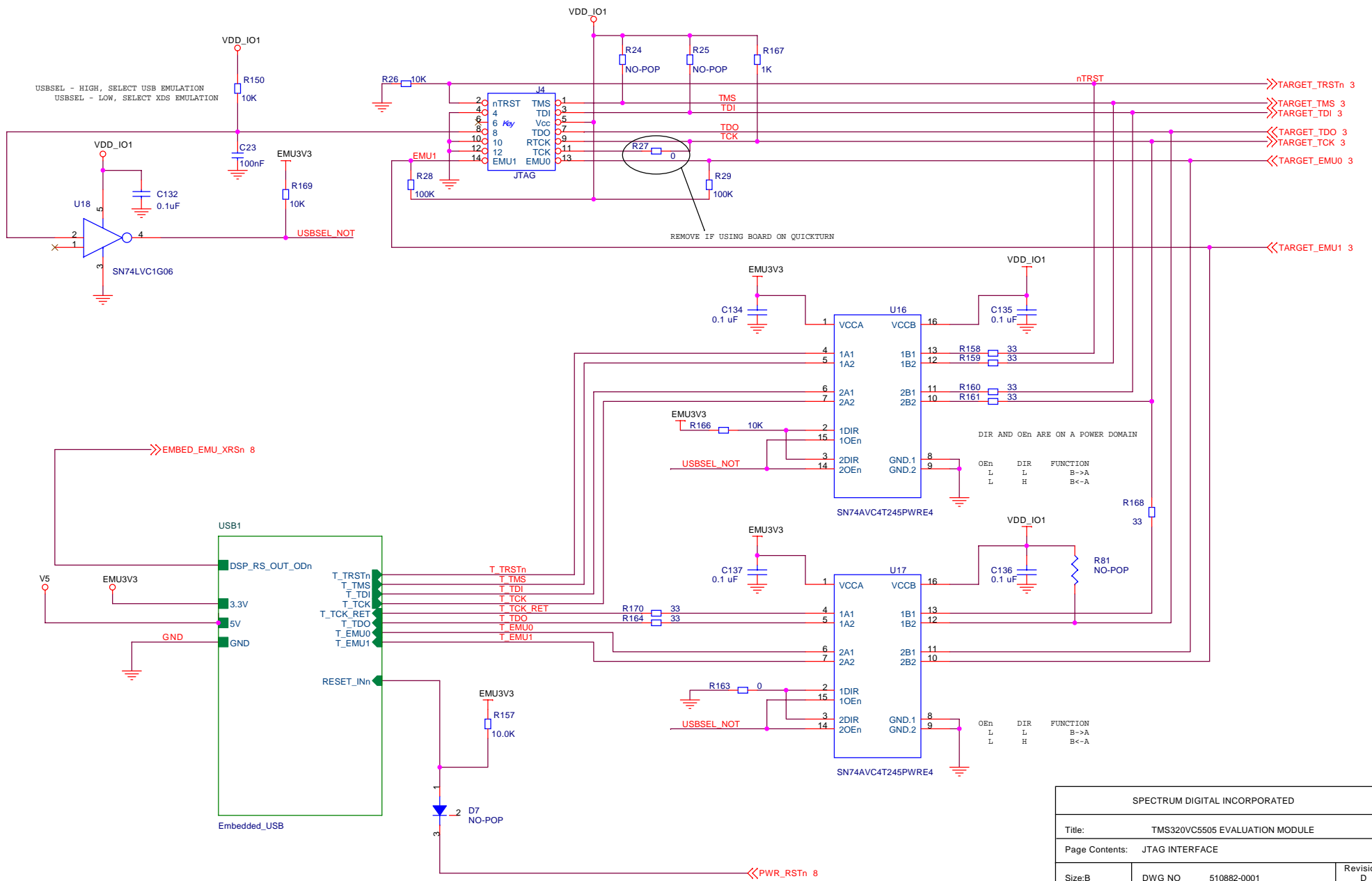


Place as close as possible to R10

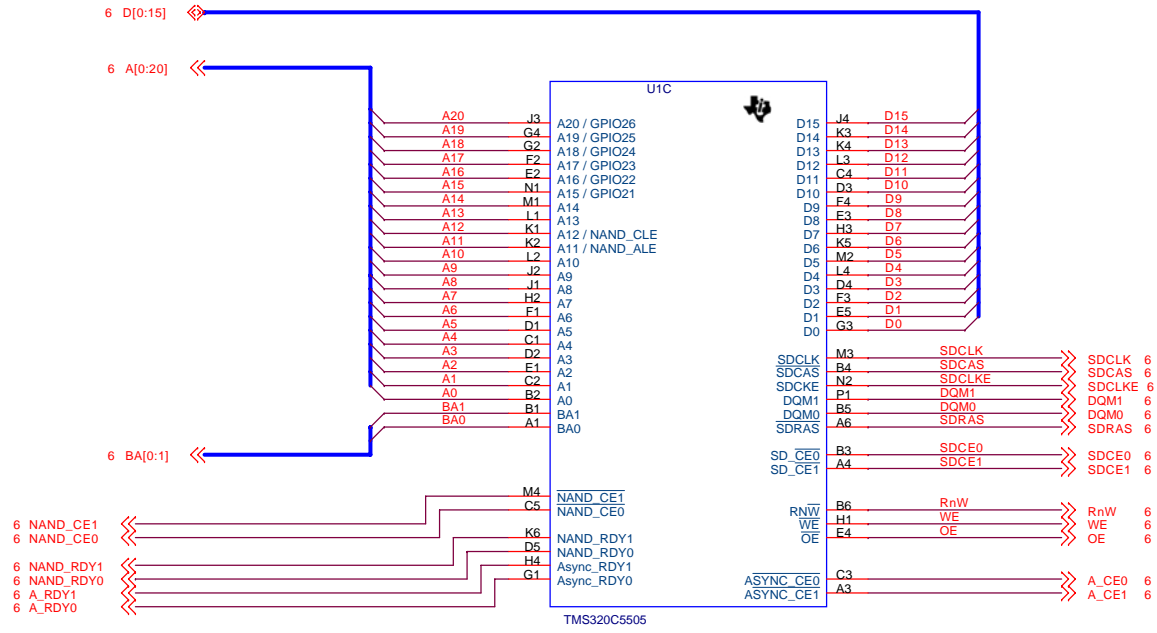
PLACE CLOSE TO U1 TCK PIN

DIR=H : A to B
DIR=L : B to A

SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: CLOCK,JTAG,USB			
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Page Contents: C5505 EMIF			
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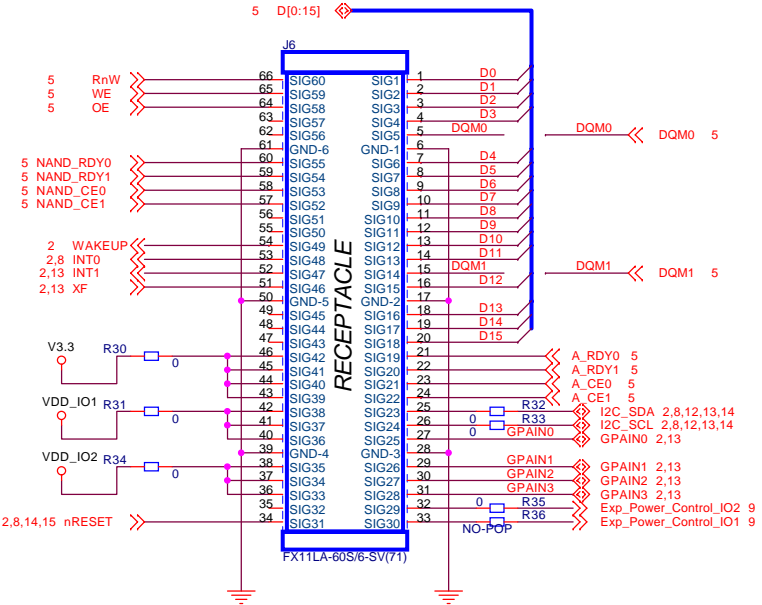
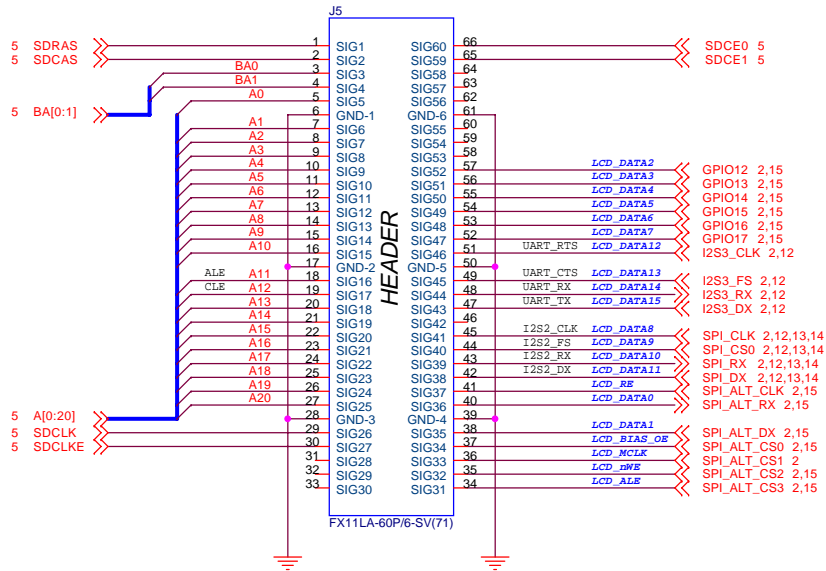
5

4

3

2

1



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: EMIF EXPANSION CONNECTORS			
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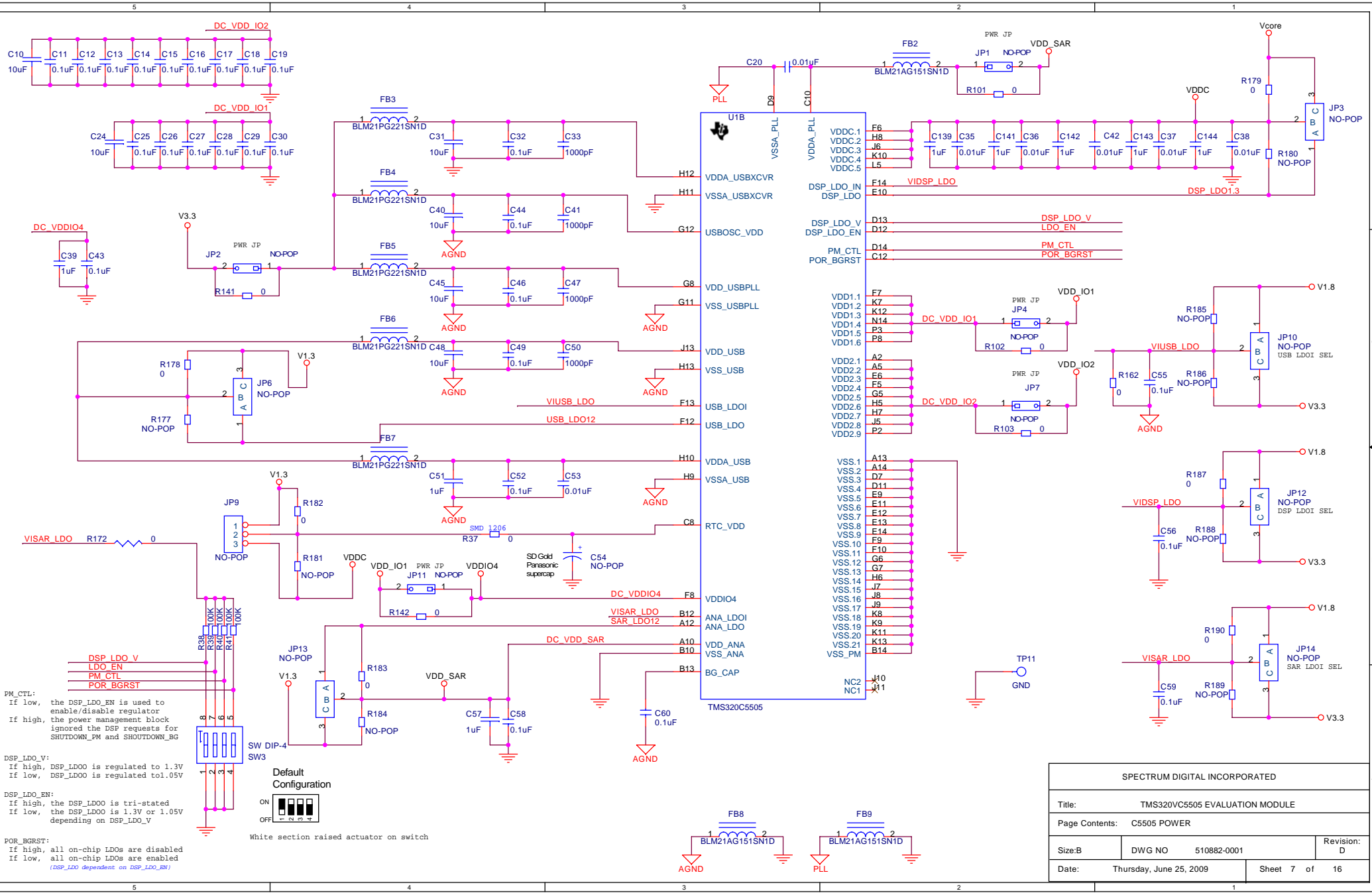
5

4

3

2

1

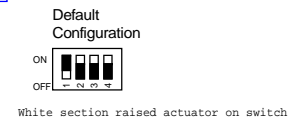


PM_CTL:
If low, the DSP_LDO_EN is used to enable/disable regulator
If high, the power management block ignored the DSP requests for SHUTDOWN_PM and SHUTDOWN_BG

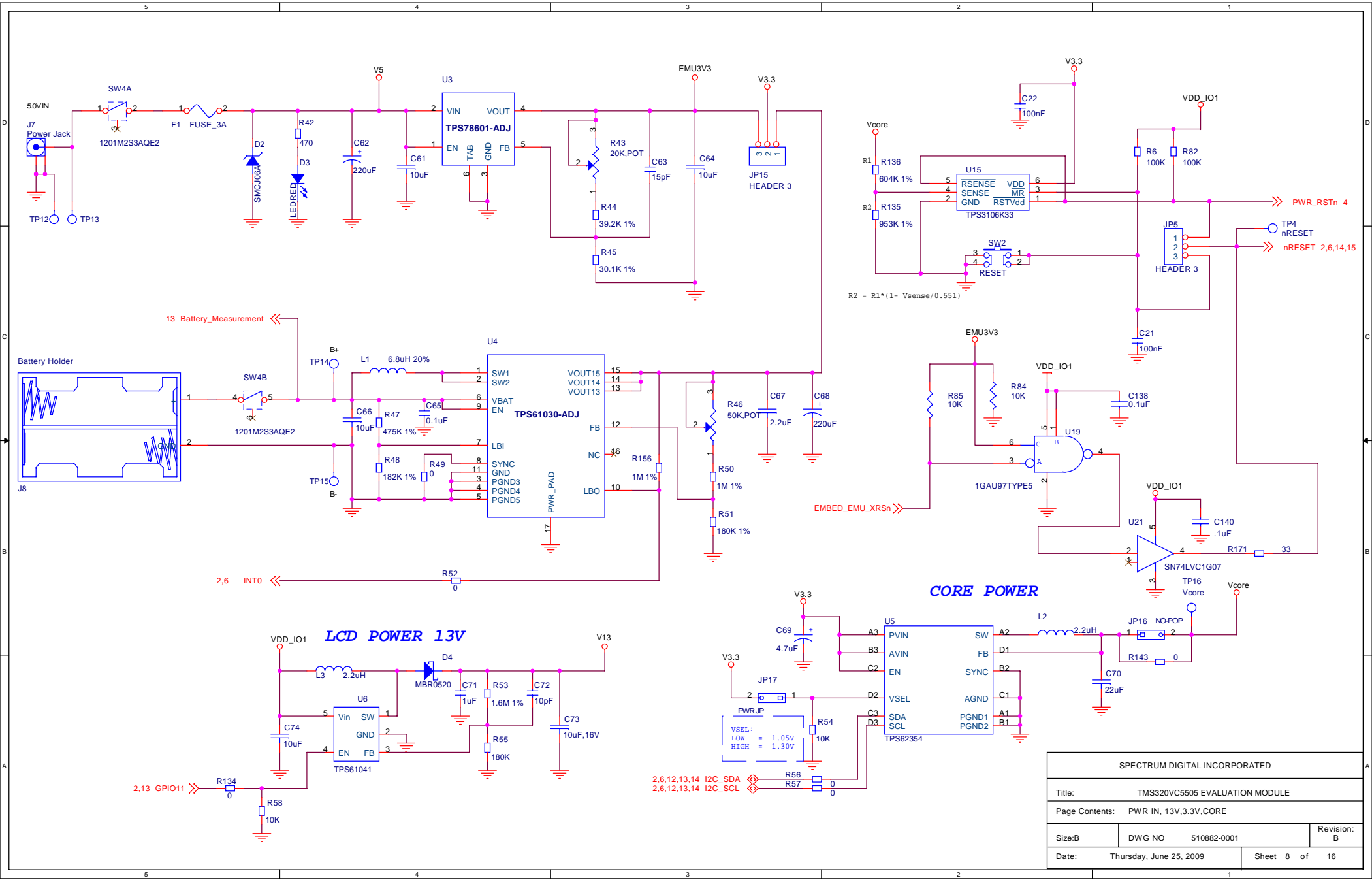
DSP_LDO_V:
If high, DSP_LDO0 is regulated to 1.3V
If low, DSP_LDO0 is regulated to 1.05V

DSP_LDO_EN:
If high, the DSP_LDO0 is tri-stated
If low, the DSP_LDO0 is 1.3V or 1.05V depending on DSP_LDO_V

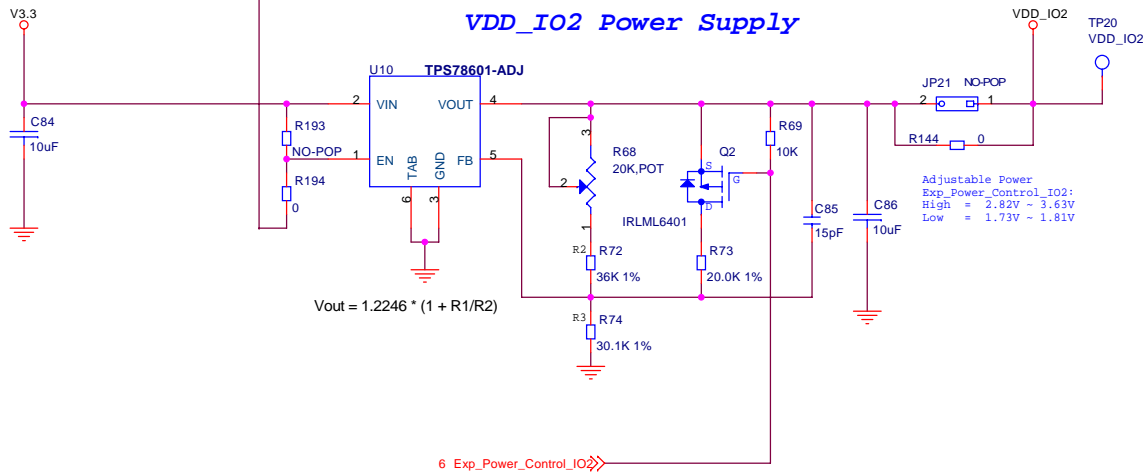
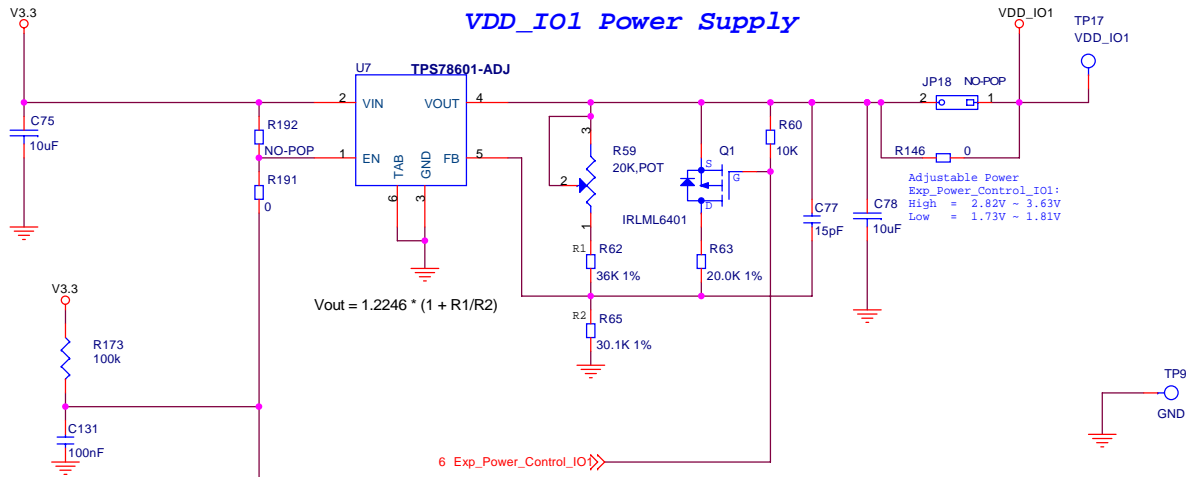
POR_BGRST:
If high, all on-chip LDOs are disabled
If low, all on-chip LDOs are enabled
(DSP_LDO dependent on DSP_LDO_EN)



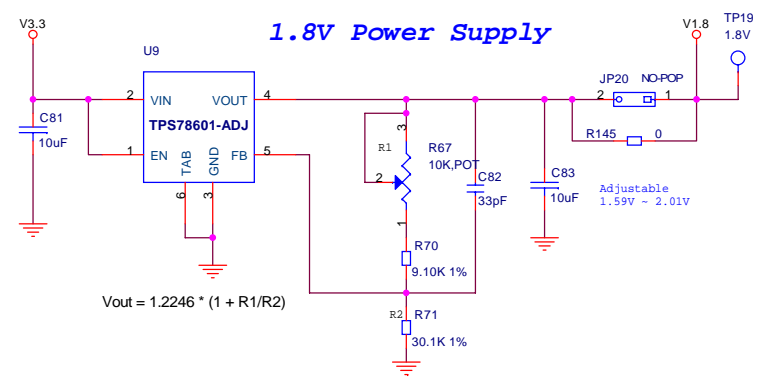
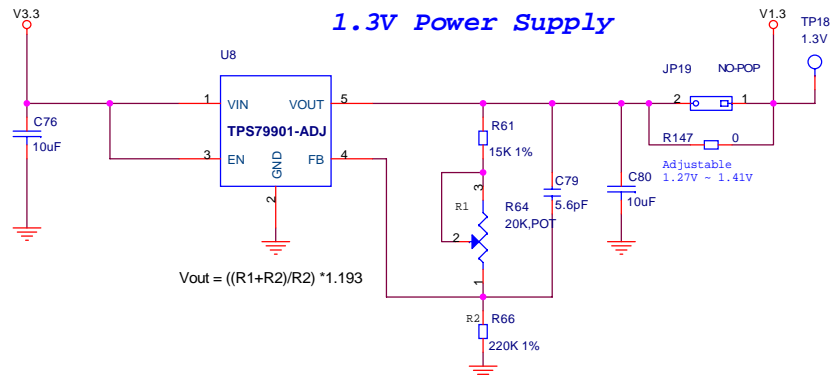
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: C5505 POWER			
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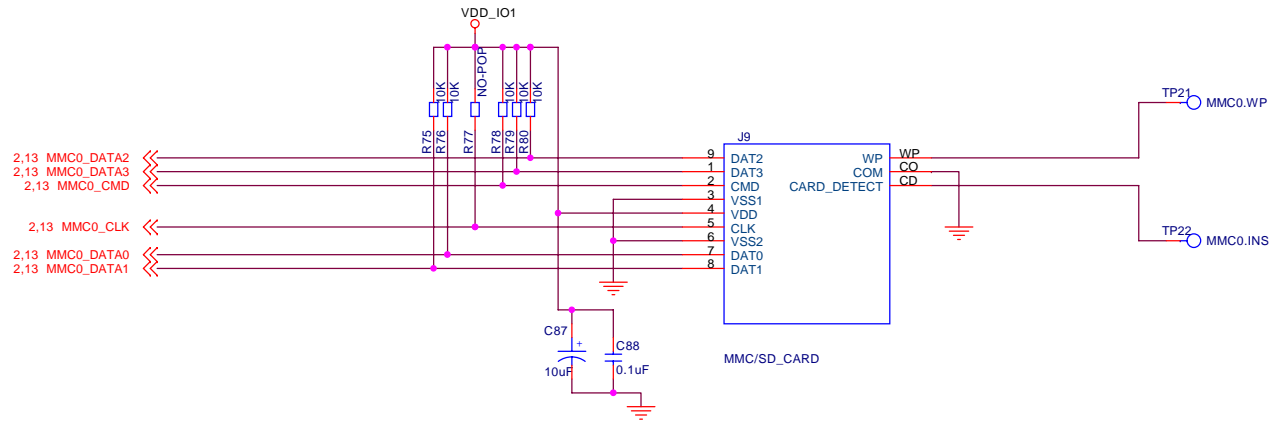
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: PWR IN, 13V, 3.3V, CORE			
Size: B	DWG NO	510882-0001	Revision: B
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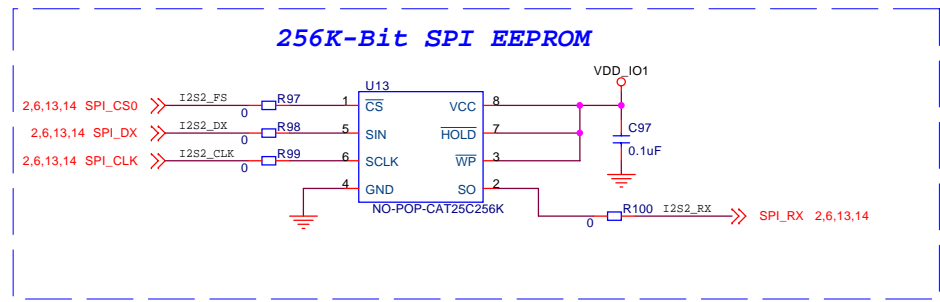
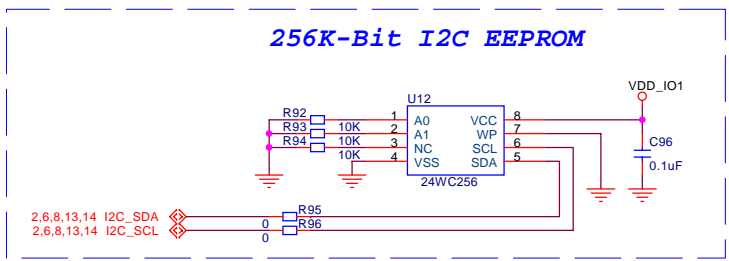
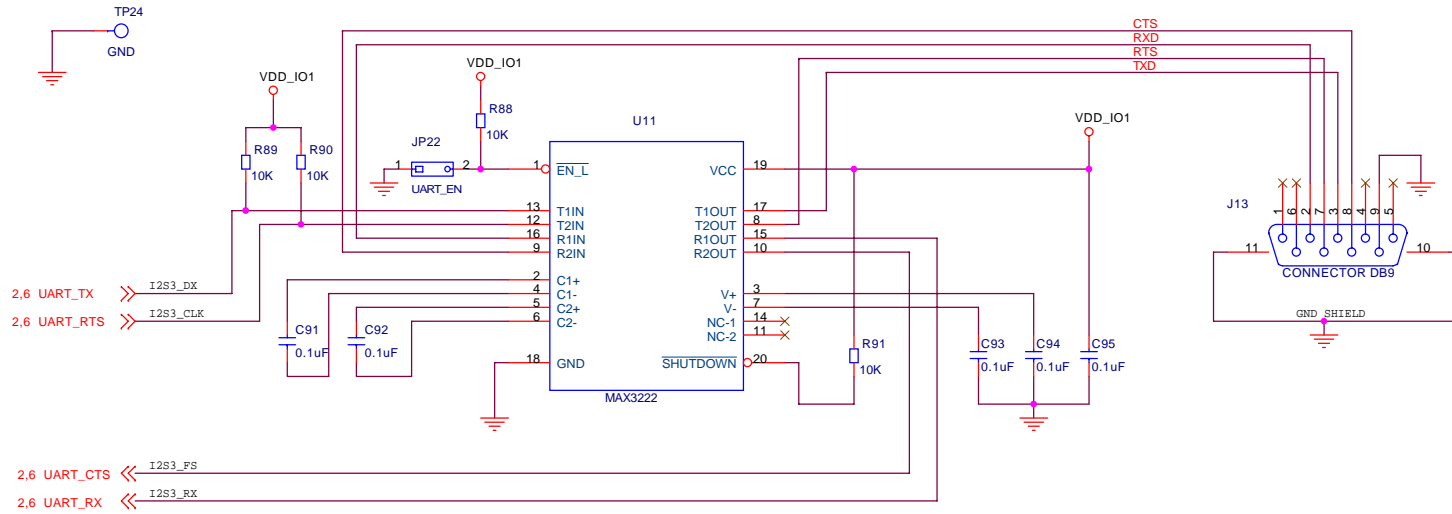
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: VDD_IO1, VDD_IO2			
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Page Contents: PWR IN, 1.3V, 1.8V, VDDIO			
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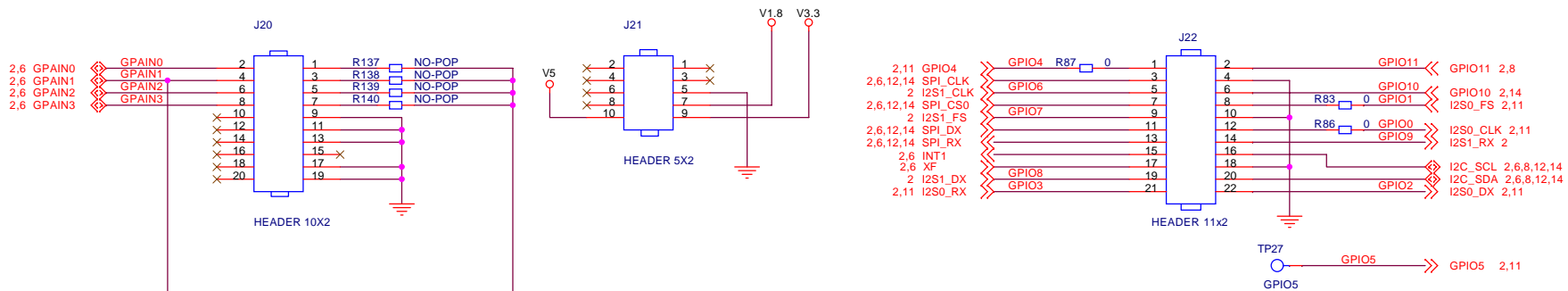
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: MMC/SD SOCKETS			
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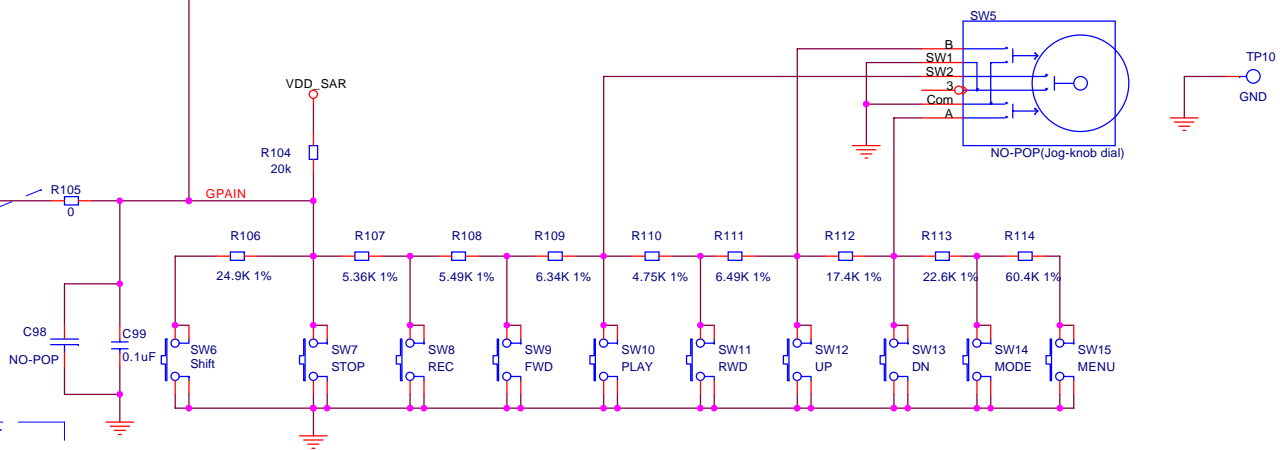
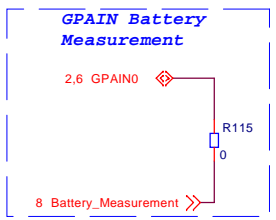
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: RS232(UART)/EEPROM			
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LAYOUT NOTE:

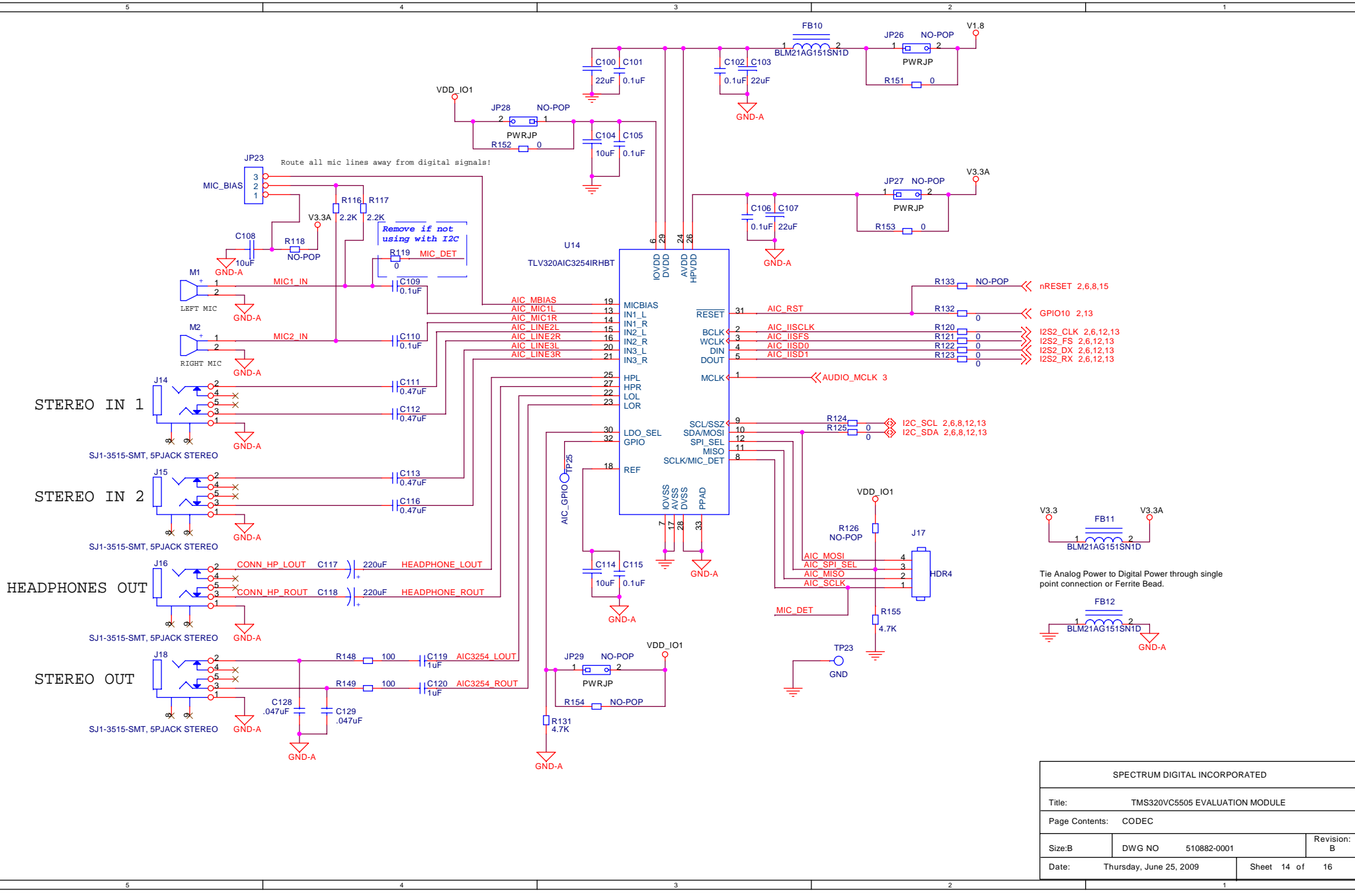
These 3 connectors need to be placed in specific coordinates to allow for Interfacing to the ADS Codec Daughter Card



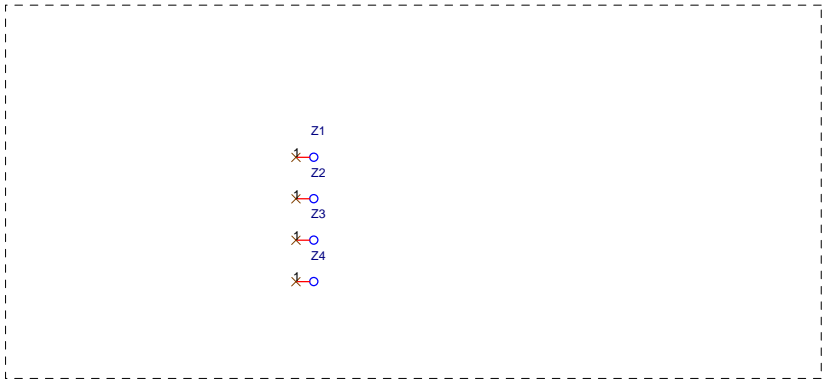
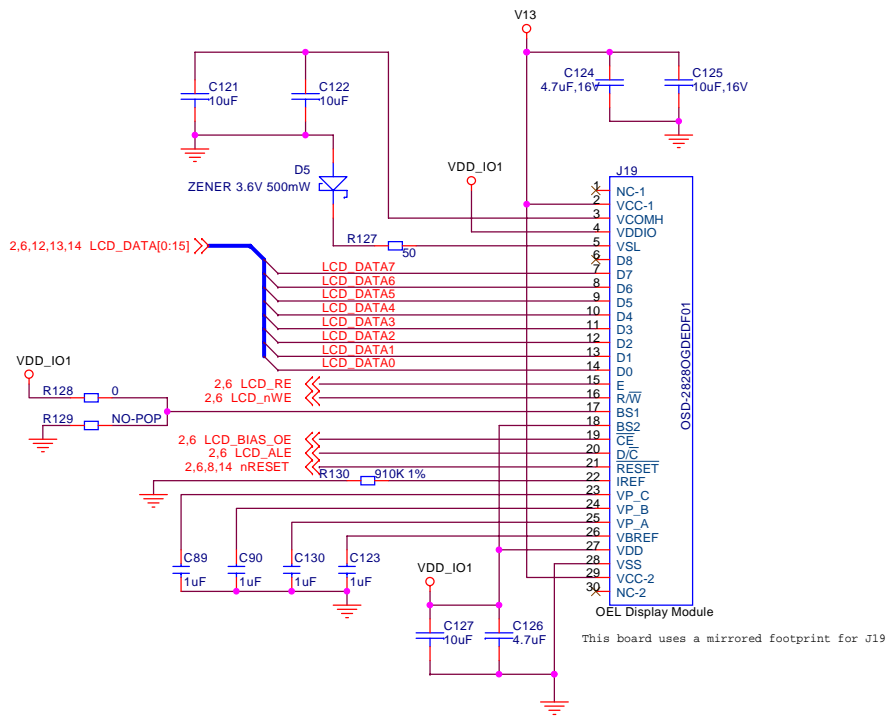
Remove R105 for Internal Voltage Measurement



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Page Contents: SAR RESISTOR NETWORK			
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Page Contents: CODEC			
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Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: COLOR LCD INTERFACE			
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Revision	DESCRIPTION	DATE
510540-0001B	Initial Release. Updated Known bugs and notes on pages 2 and 6	12/26/07 01/08/08
510880-0001A	<ol style="list-style-type: none"> 1. Change R50 to 1M 2. Fix power on LCD connector. Swap 3.3V with 13V 3. Fix ball F8 to be used as VSS_OSC 4. Fix INIT0 and INIT1 (swapped) 5. Fix CODEC so that I2C is selected by default 6. Changed connection to R16 to USB_XO instead of USB_XI 7. Replaced J22 with 11x2 (same xy on pin 1) 8. Replaced I2S on J22 with SPI 9. Added test pin to GPIO5 10. Changed value of R62, R72 to 36K 11. Added Embedded USB emulation option 	02/18/08
510880-0001B	<ol style="list-style-type: none"> 1. Fixed Jog-Dial so that common dial switches ties to gnd 2. Fixed pull-up resistor net connected to DSP_LDO_V and LDO_EN 	03/09/08
510880-0001C	<ol style="list-style-type: none"> 1. NEW CPU REVISION 2. ECN ON R21 3. R13 CHANGED TO 0 OHM 4. C54 NOT POPULATED 5. C60 CHANGED TO 0.1uF 	12/09/08
510880-0001D	<ol style="list-style-type: none"> 1. NEW CPU REVISION 2. MODIFIED POWER SEQUENCING 	

SPECTRUM DIGITAL INCORPORATED			
Title: TMS320VC5505 EVALUATION MODULE			
Page Contents: REVISION SUMMARY			
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