

SCHEMATIC CONTENTS

NOTES, UNLESS OTHERWISE SPECIFIED:

- RESISTANCE VALUES IN OHMS.
- CAPACITANCE VALUES IN MICROFARADS.
- LAST REFERENCE DESIGNATORS :
- ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
- OBSERVE THE FOLLOWING LAYOUT NOTES:
 - FOLLOW USB APNOTE GUIDELINES
 - FOLLOW DDR2 APNOTE GUIDELINES
- BOARD PROPERTIES
 - ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE

B1. General layers 50 +/- 5 OHM MATCHED IMPEDANCE

B2. USB layer 90 ohm differential

- OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
- INNER LAYERS 1.0 OZ CU
- FR4 BOARD MATERIAL
- MINIMUM TRACE WIDTH/SPACING 4 MILS
- MINIMUM VIA SIZE 10/19 MIL
- LAYER STACKUP:
 - TOP - SIGNAL ROUTING
 - GROUND PLANE
 - INNER1 - SIGNAL ROUTING
 - GROUND PLANE
 - INNER2 - SIGNAL ROUTING
 - INNER3 - SIGNAL ROUTING
 - VCC PLANE 1
 - VCC PLANE 2
 - INNER4 - SIGNAL ROUTING
 - INNER5 - SIGNAL ROUTING
 - GROUND PLANE
 - INNER5 - SIGNAL ROUTING
 - GROUND PLANE
 - BOTTOM - SIGNAL ROUTING

SHEET01 - TITLE
 SHEET02 - JTAG EMULATION CONNECTORS
 SHEET03 - DSP CLKS/RST/EMU
 SHEET04 - DSP SERIAL I/O
 SHEET05 - DSP USBII
 SHEET06 - DSP EMIF/PCI
 SHEET07 - DSP DDR Interface
 SHEET08 - DSP VIDEO Ports
 SHEET09 - DSP ENET

SHEET10 - DSP POWER PINS
 SHEET11 - DSP DECOUPLING CAPS
 SHEET12 - BOOT DIP SWITCHES
 SHEET13 - I2C EXP,SPI EEPROM, I2C ROMS
 SHEET14 - DDR2 MEMORIES
 SHEET15 - NAND-FLASH
 SHEET16 - CONTROL LOGIC
 SHEET17 - ENET DAUGHTER CARD CONN
 SHEET18 - ENETCONTROLLER
 SHEET19 - ENET POWER

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 SHEET21 - RS232/IR RECEIVER
 SHEET22 - USBII INTERFACE
 SHEET23 - ATA INTERFACE
 SHEET24 - PCI-MUX
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 SHEET26 - PCI-CONNECTOR
 SHEET27 - VLYNQ CONNECTOR
 SHEET28 - AIC32
 SHEET29 - SPDIF

SHEET30 - VIDEO CLOCKS
 SHEET31 - VIDEO INPUT MUXING
 SHEET32 - TVP7002
 SHEET33 - TVP5147 COMPOSITE
 SHEET34 - TVP5147 II S-VIDEO
 SHEET35 - VIDEO OUTPUT MUXING
 SHEET36 - ADV7343
 SHEET37 - COMPOSITE/S-VIDEO BUFFERING
 SHEET38 - COMPONENT VIDEO BUFFERING
 SHEET39 - VIDEO DAUGHTER CARD CONN

SHEET40 - I/O DAUGHTER CARD CONN
 SHEET41 - DSP CORE POWER
 SHEET42 - POWER 1V8, 3V3
 SHEET43 - POWER IN, RESET SUPERVISOR

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic for layout	04/30/07	RRP
B	Initial schematic updated after initial pwb build	05/25/07	RRP
C	PRE-PRODUCTION RELEASE	07/05/07	RRP
D	ADV7343 CHANGE TO INTERNAL REFERENCE	08/15/07	RRP

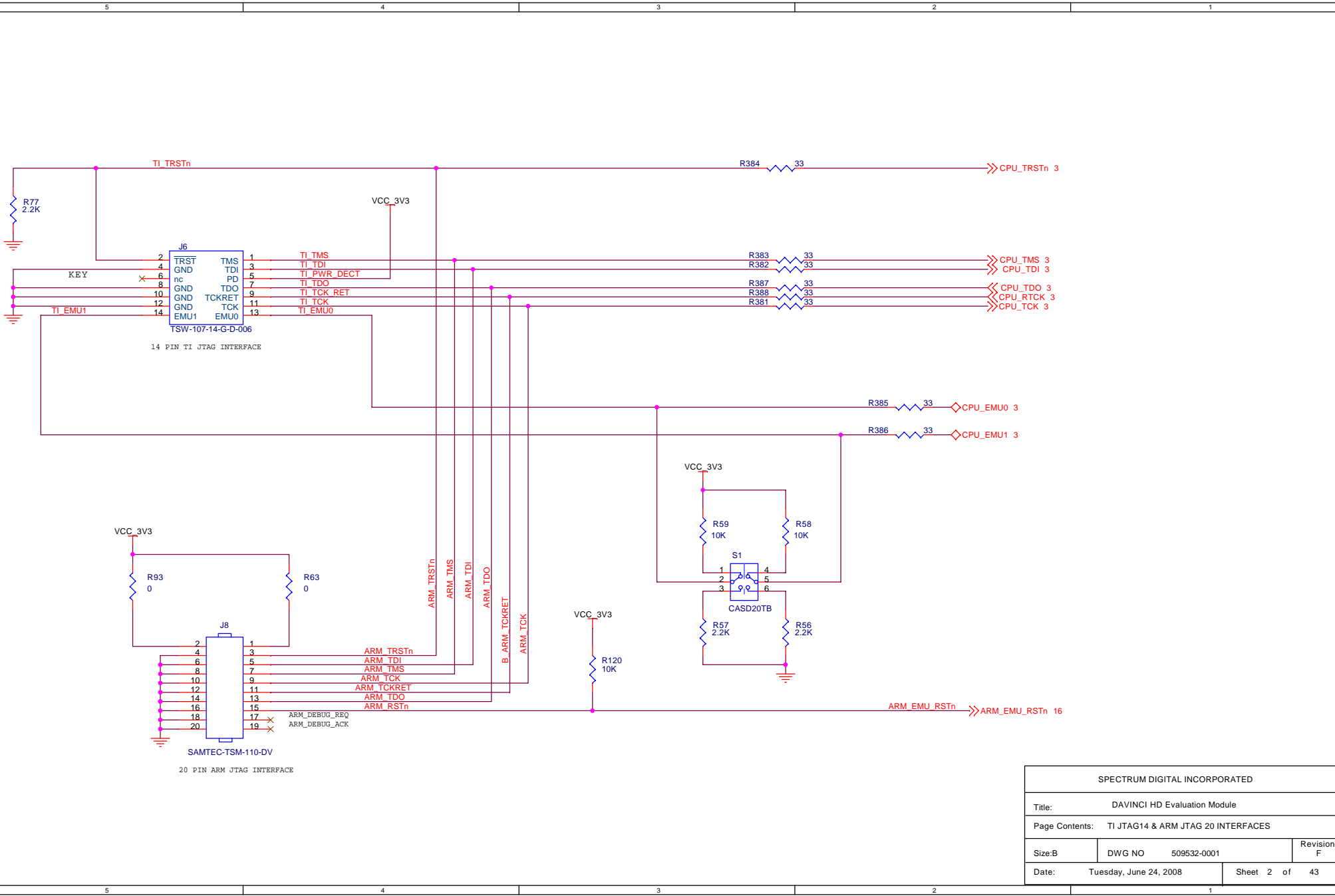
ADDRESS	DESCRIPTION
0000 0000	MEMORY MAP
	ARM RAM
3000 0000	PCI ADDRESS SPACE
4200 0000	NAND FLASH EMCS2
4C00 0000	VLYNQ REMOTE DEVICES
8000 0000	DDR2 RAM - 256 Megabytes (1st half of 512 Megabytes)
A000 0000	DDR2 RAM - (512 Megabytes optional)
C000 0000	RESERVED

I2C ADDRESS MAP		
BASE	I2C ADDRESS TABLE	SHEET
0x50	I2C ROM	13
0x18	AIC32	28
0x5D	TVP5147 I	33
0x5C	TVP5147 II	34
0x38	IO EXPANDER 0 (LEDS/USER_SW)	13
0x3A	EMBEDDED I2C REGISTER 1	16
0x3B	EMBEDDED I2C REGISTER 2	16
0x3C	EMBEDDED I2C REGISTER 3	16
0x2A	ADV7343	36
0x2C	THS7303 - OUTPUT	37
0x6C	CDCE949	30
0x5D	TVP7002	32
0x2E	THS7353 - INPUT	32

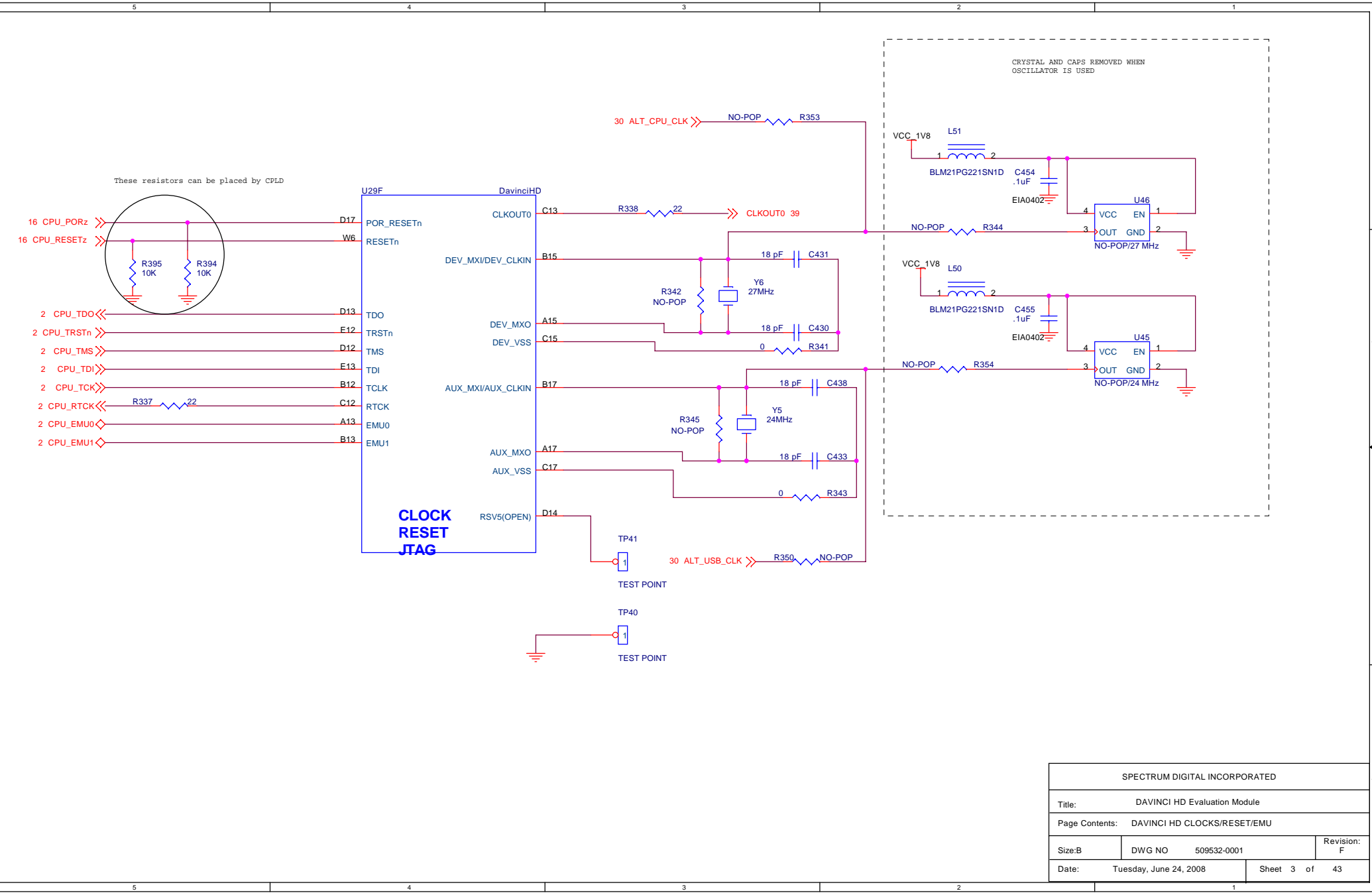
REVISION STATUS OF SHEETS									
REV	F	F	F	F	F	F	F	F	F
SH	41	42	43						

REV	F	F	F	F	F	F	F	F	F	F	DATE	BY	DESCRIPTION
SH	31	32	33	34	35	36	37	38	39	40	01/15/2007	DWN	R.R.P.
REV	F	F	F	F	F	F	F	F	F	F	01/15/2007	CHK	T.W.K.
SH	21	22	23	24	25	26	27	28	29	30	01/15/2007	ENGR	R.R.P.
REV	F	F	F	F	F	F	F	F	F	F	01/15/2007	ENGR-MGR	R.R.P.
SH	11	12	13	14	15	16	17	18	19	20	01/15/2007	QA	C.M.D.
REV	F	F	F	F	F	F	F	F	F	F	01/15/2007	MFG	R.R.P.
SH	1	2	3	4	5	6	7	8	9	10	01/15/2007	RLSE	R.R.P.

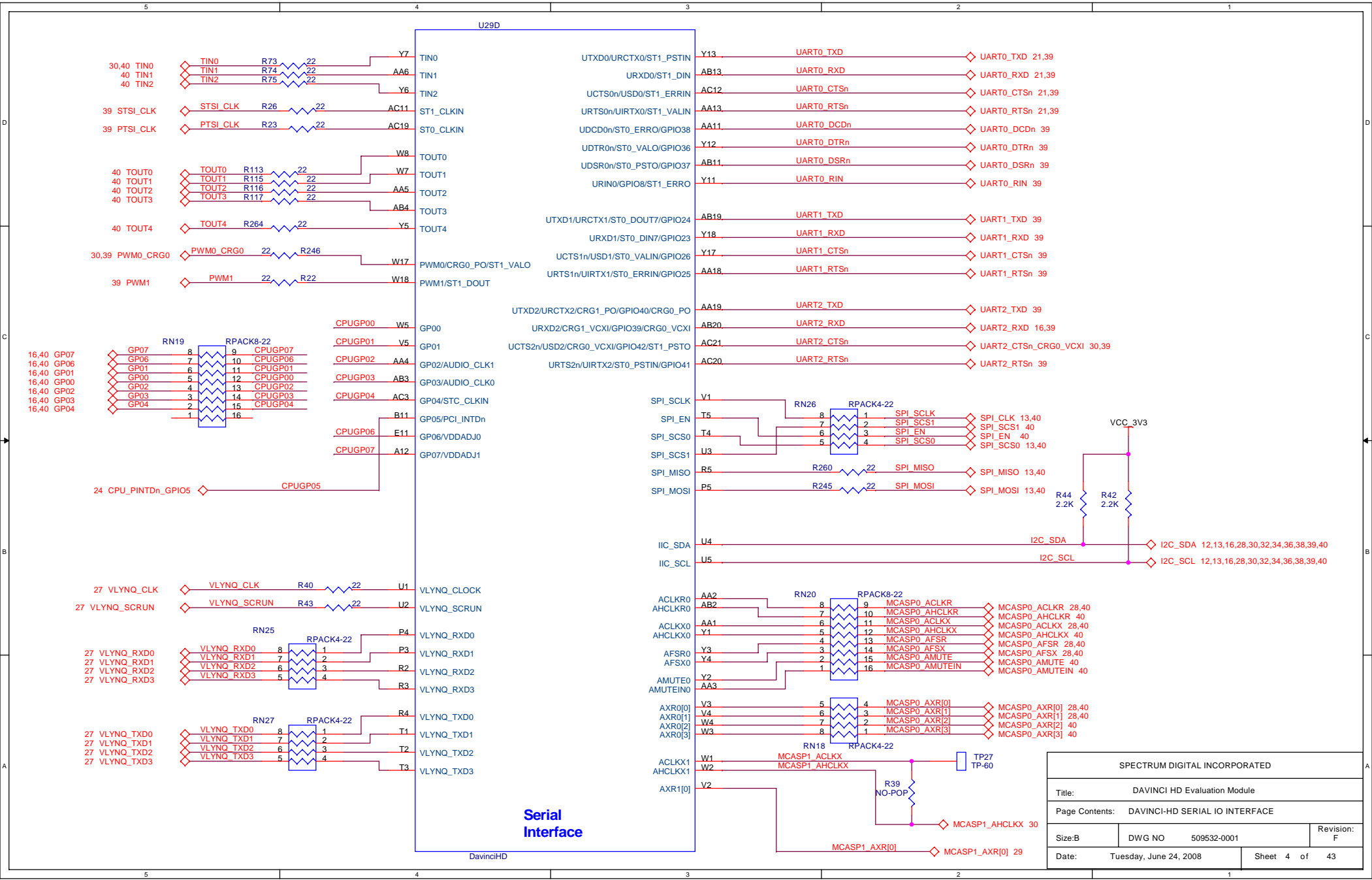
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Page Contents: TITLE SHEET			
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SPECTRUM DIGITAL INCORPORATED			
Title: DAVINCI HD Evaluation Module			
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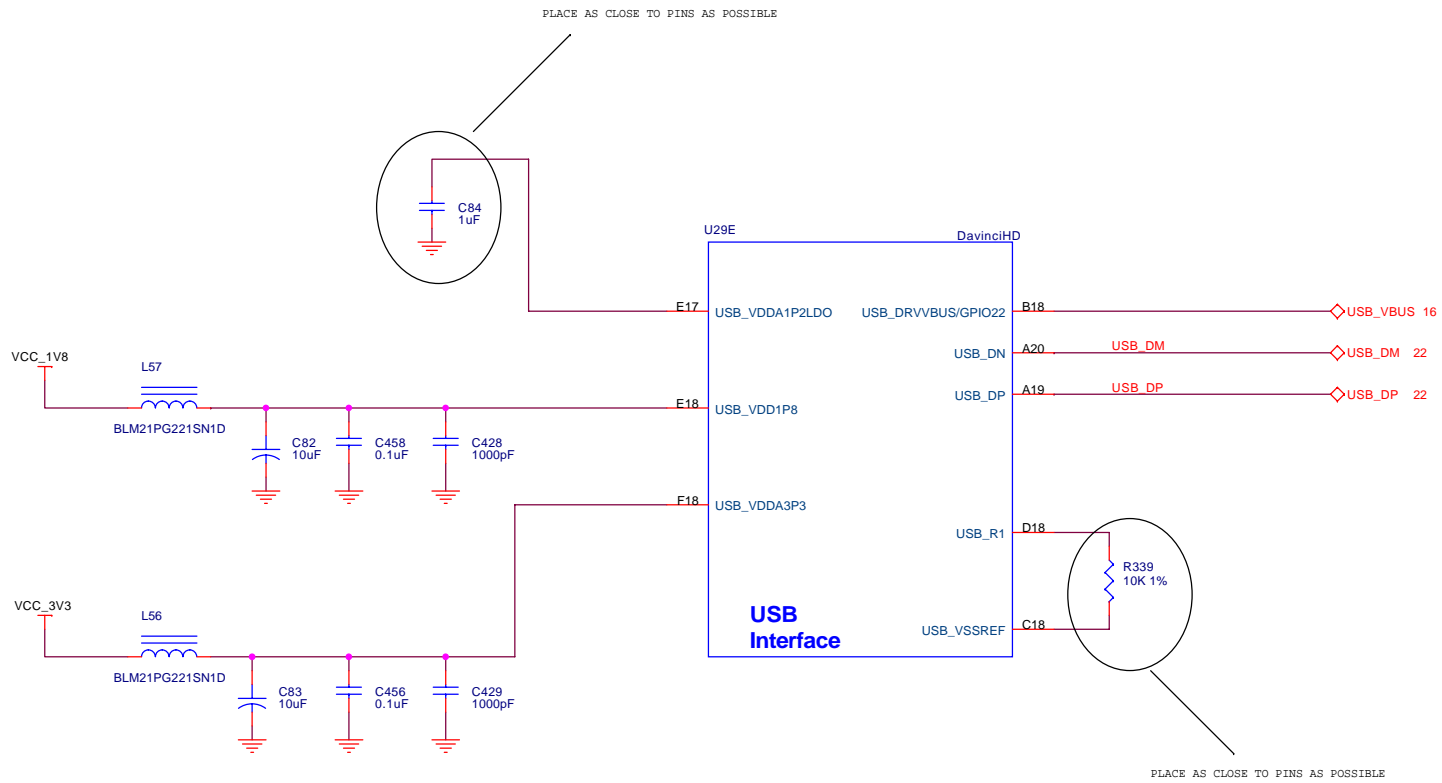
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Page Contents: DAVINCI HD CLOCKS/RESET/EMU			
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Serial Interface

DavinciHD

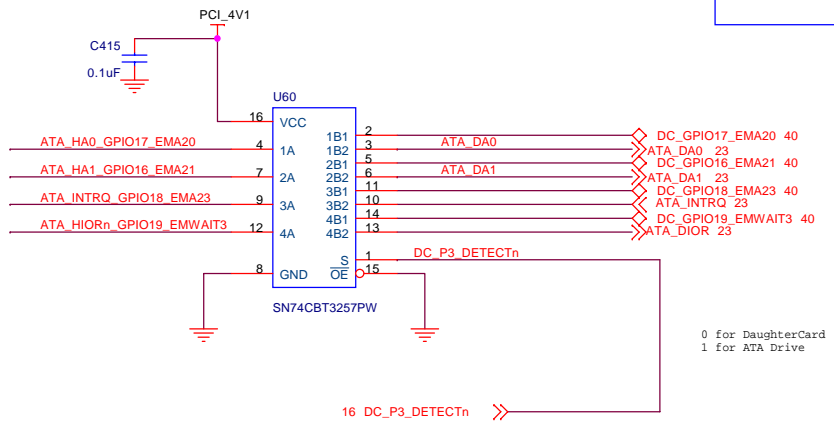
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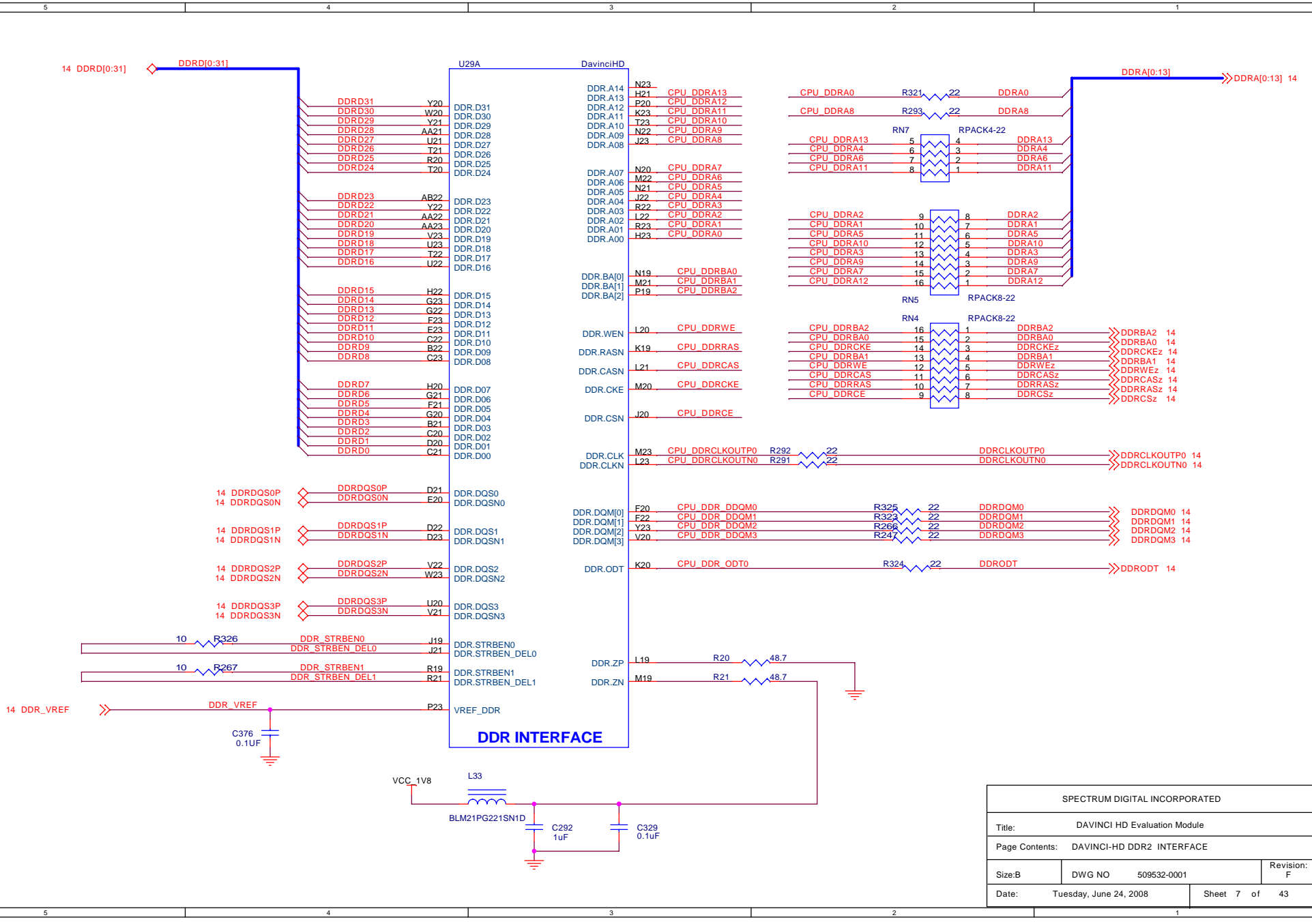
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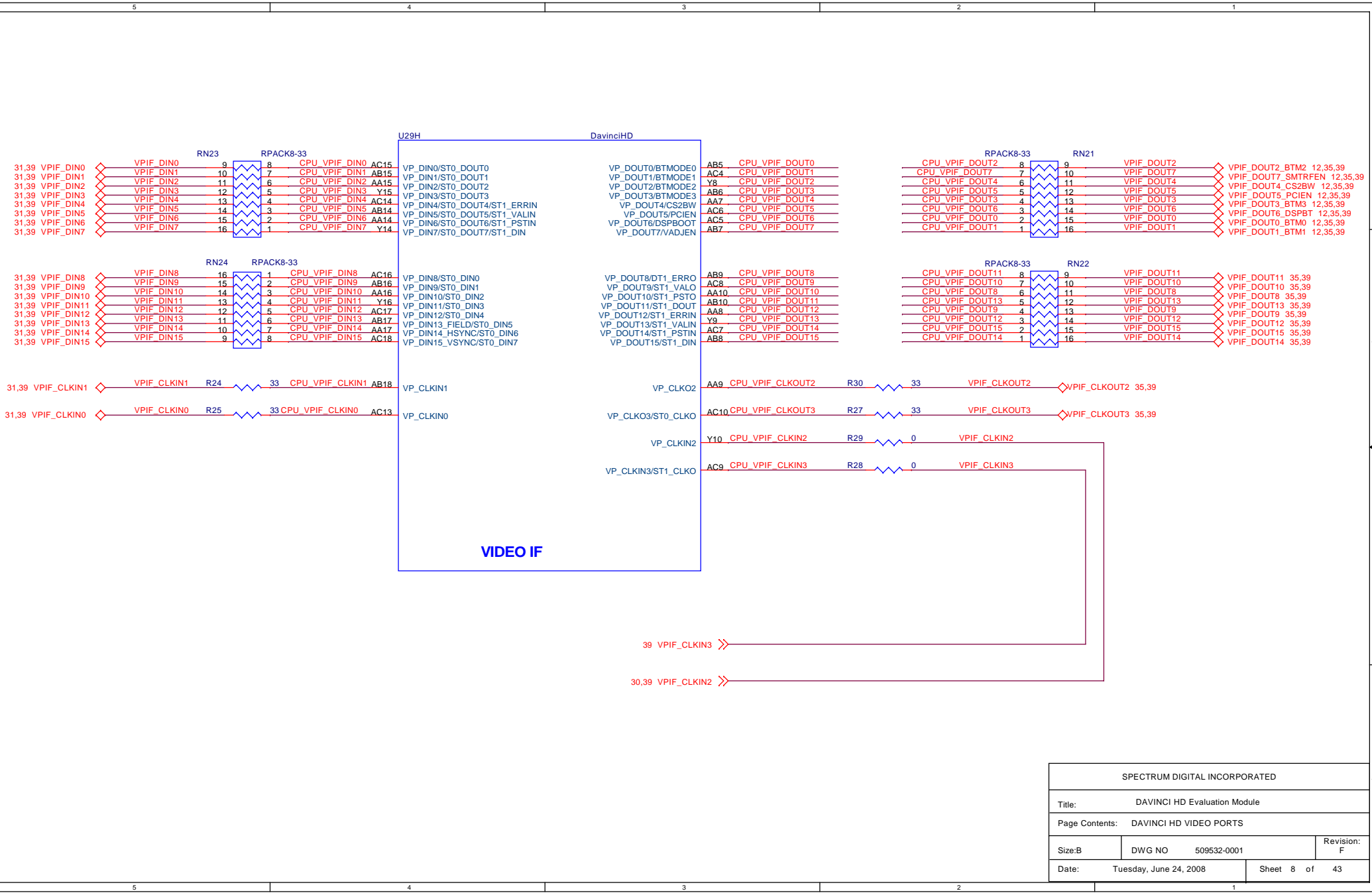
PCI



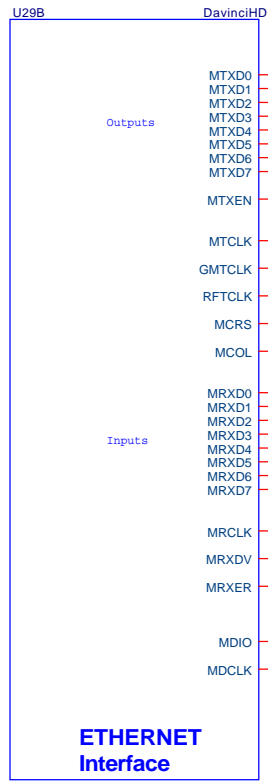
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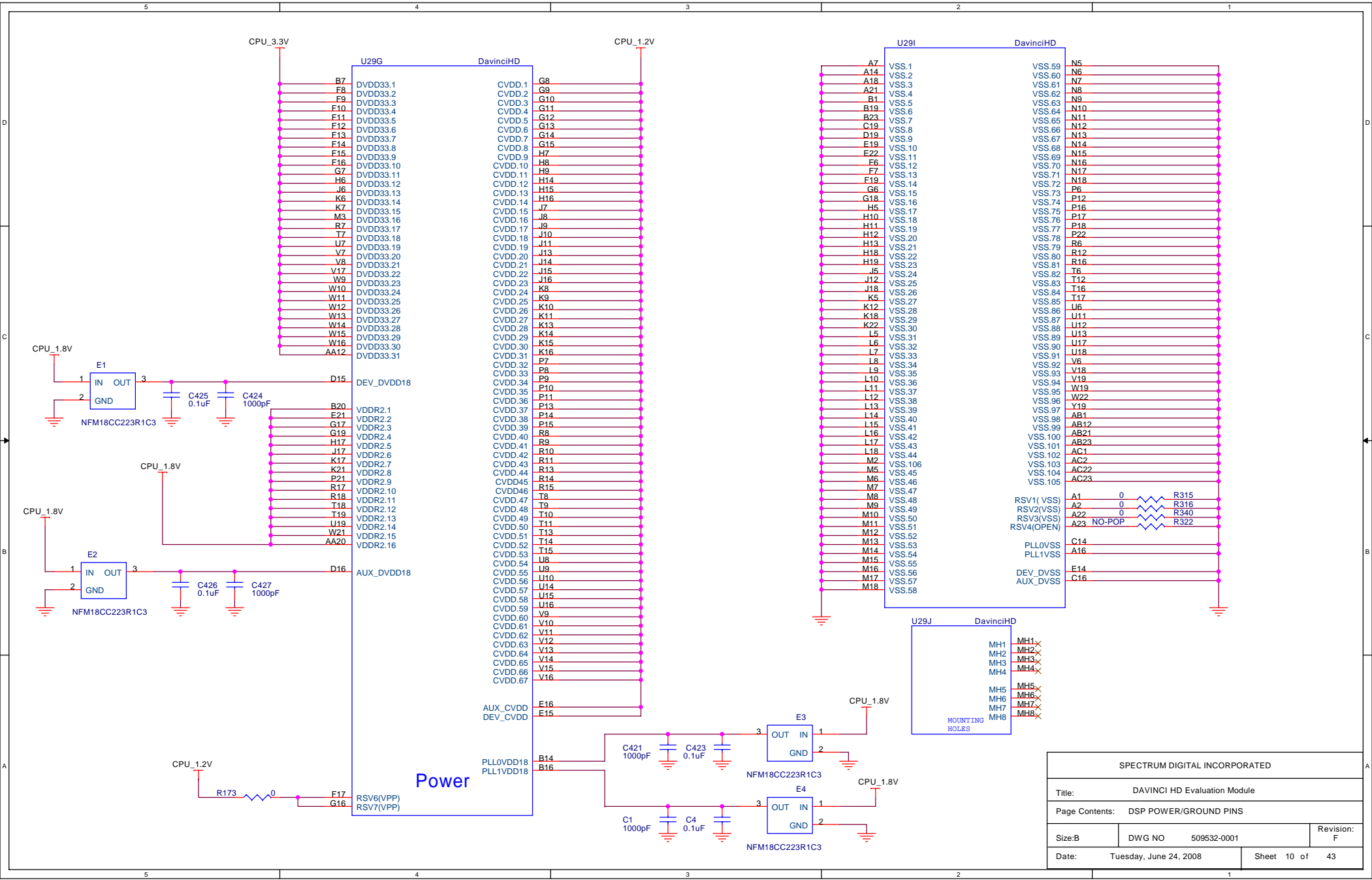


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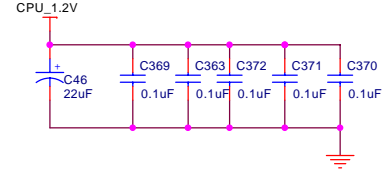
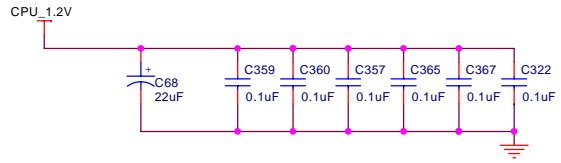
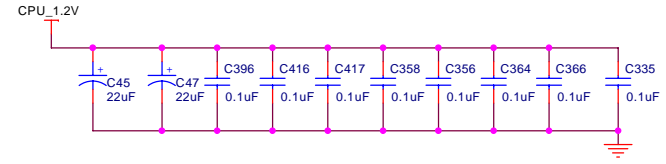
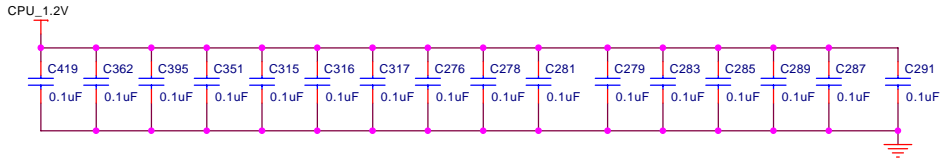
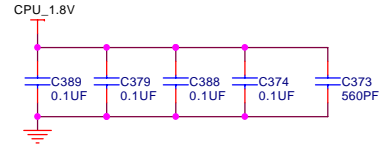
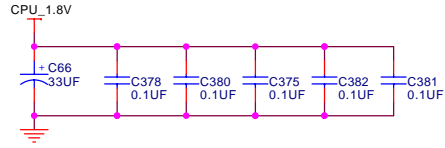
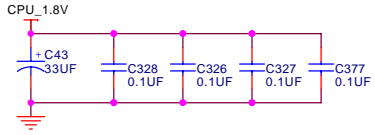
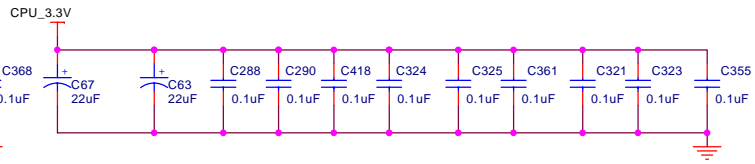
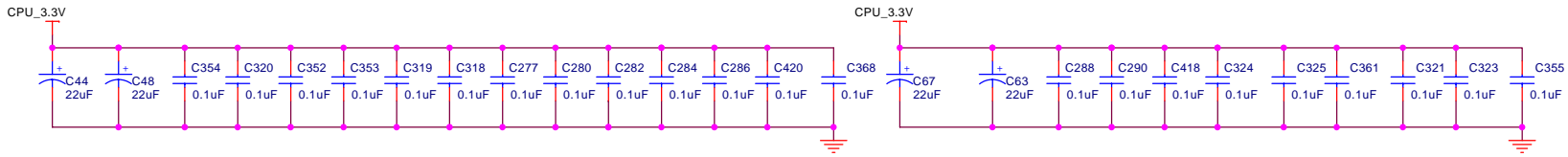


ETHERNET Interface

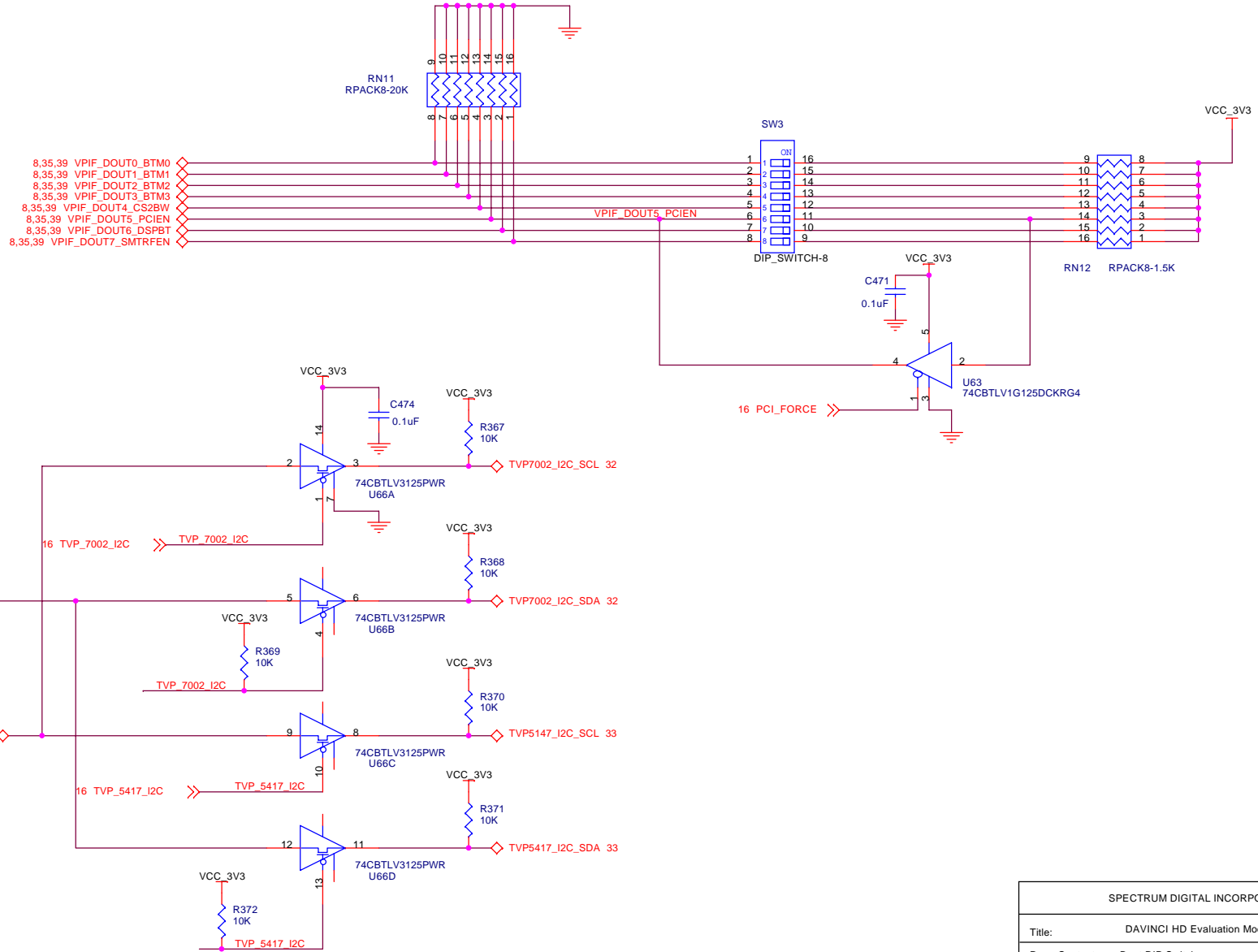
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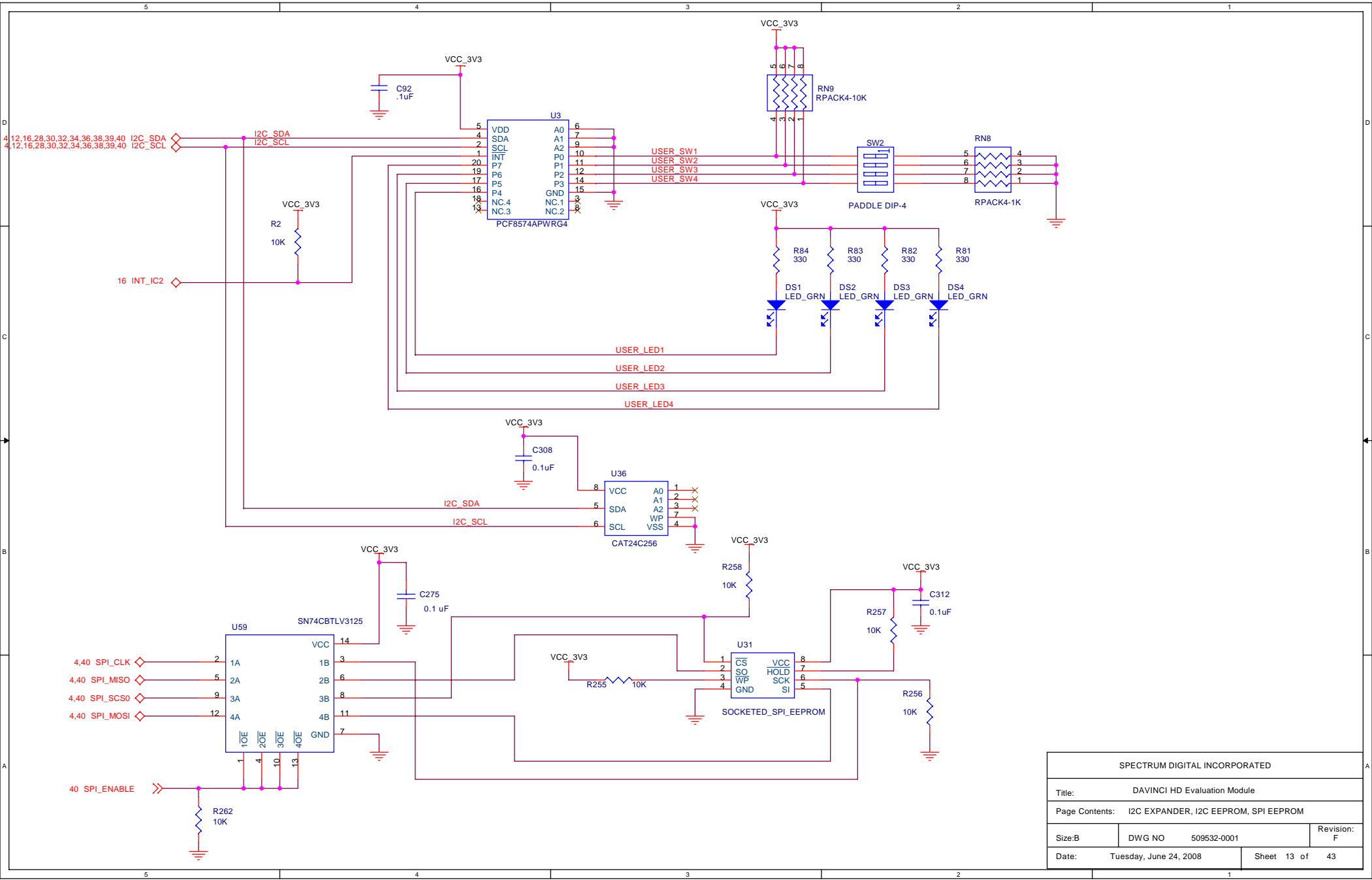
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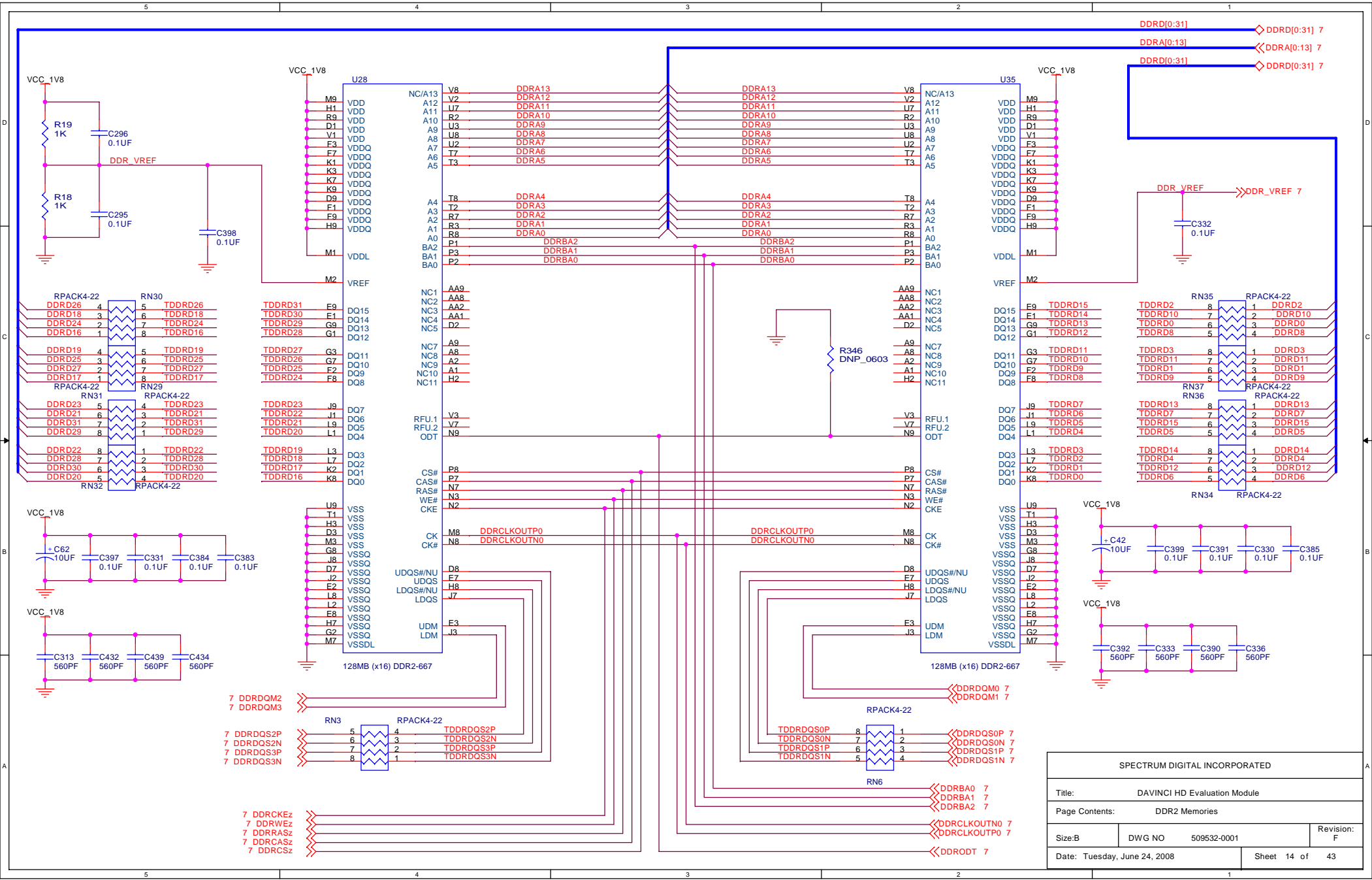
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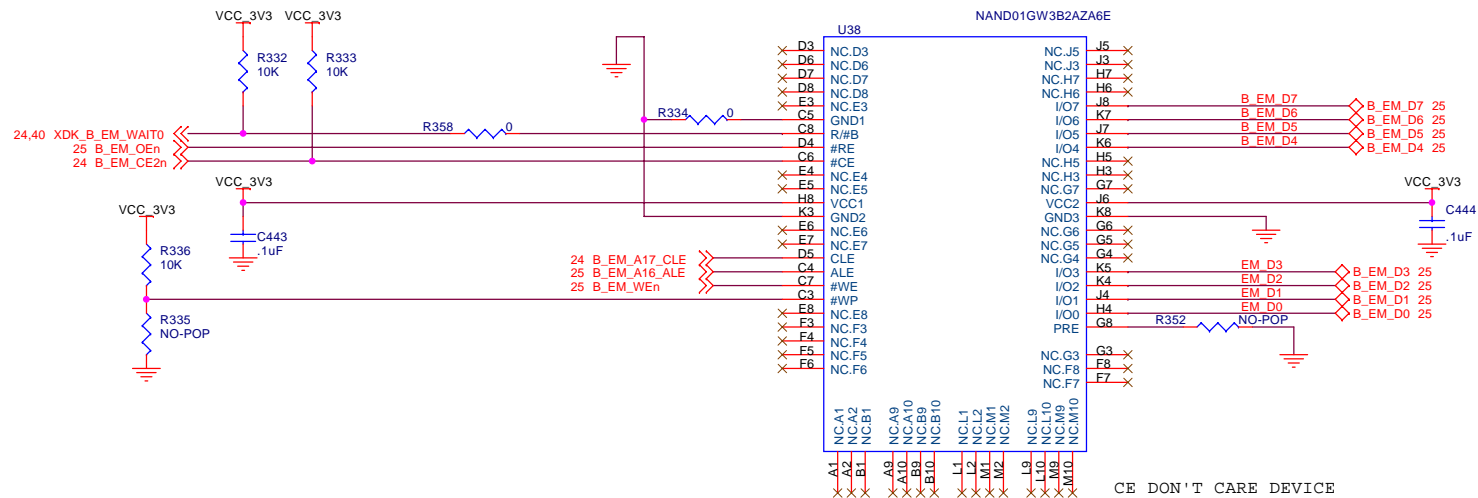
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Page Contents: Boot DIP Switches			
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Page Contents: I2C EXPANDER, I2C EEPROM, SPI EEPROM			
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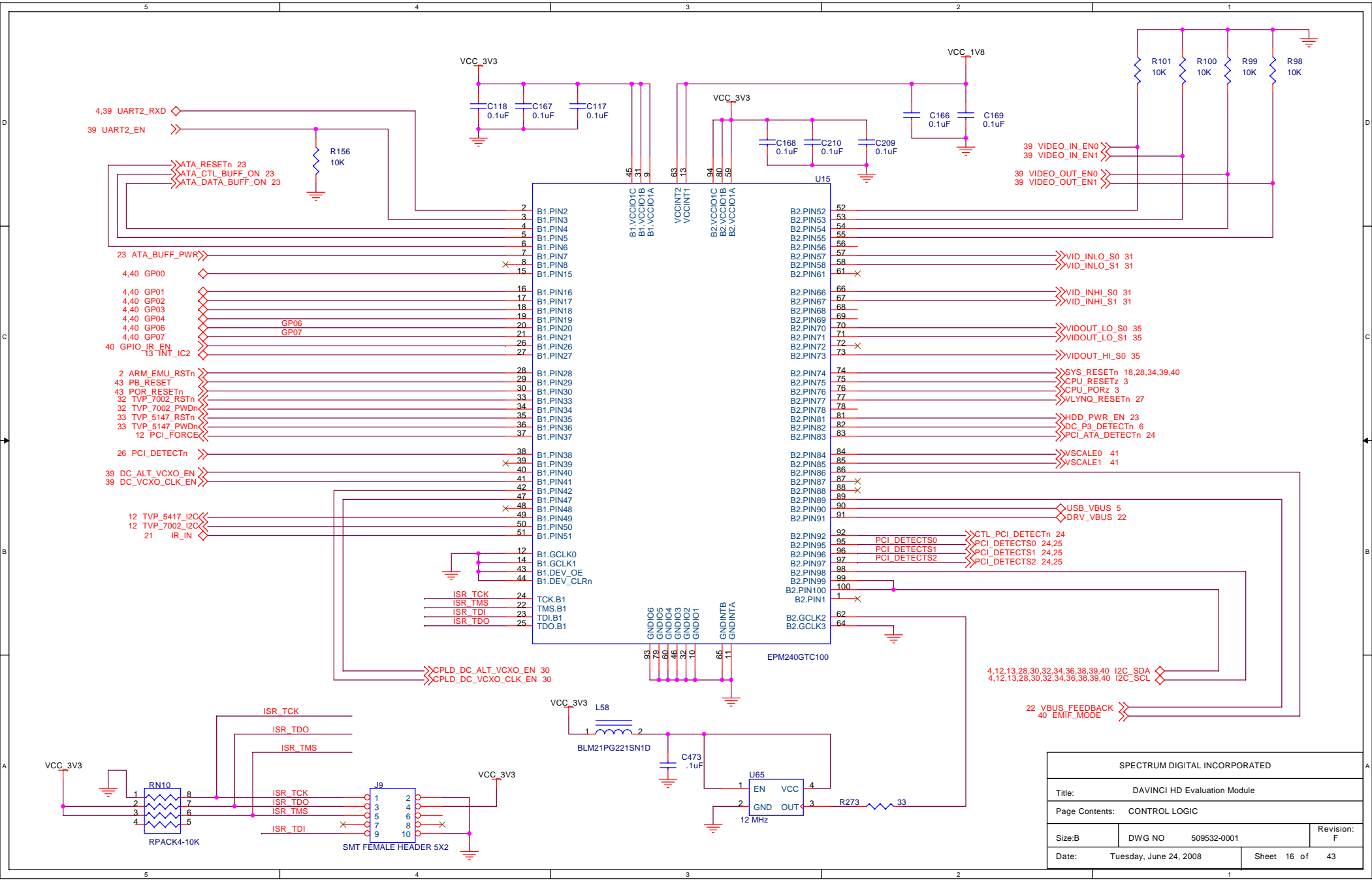


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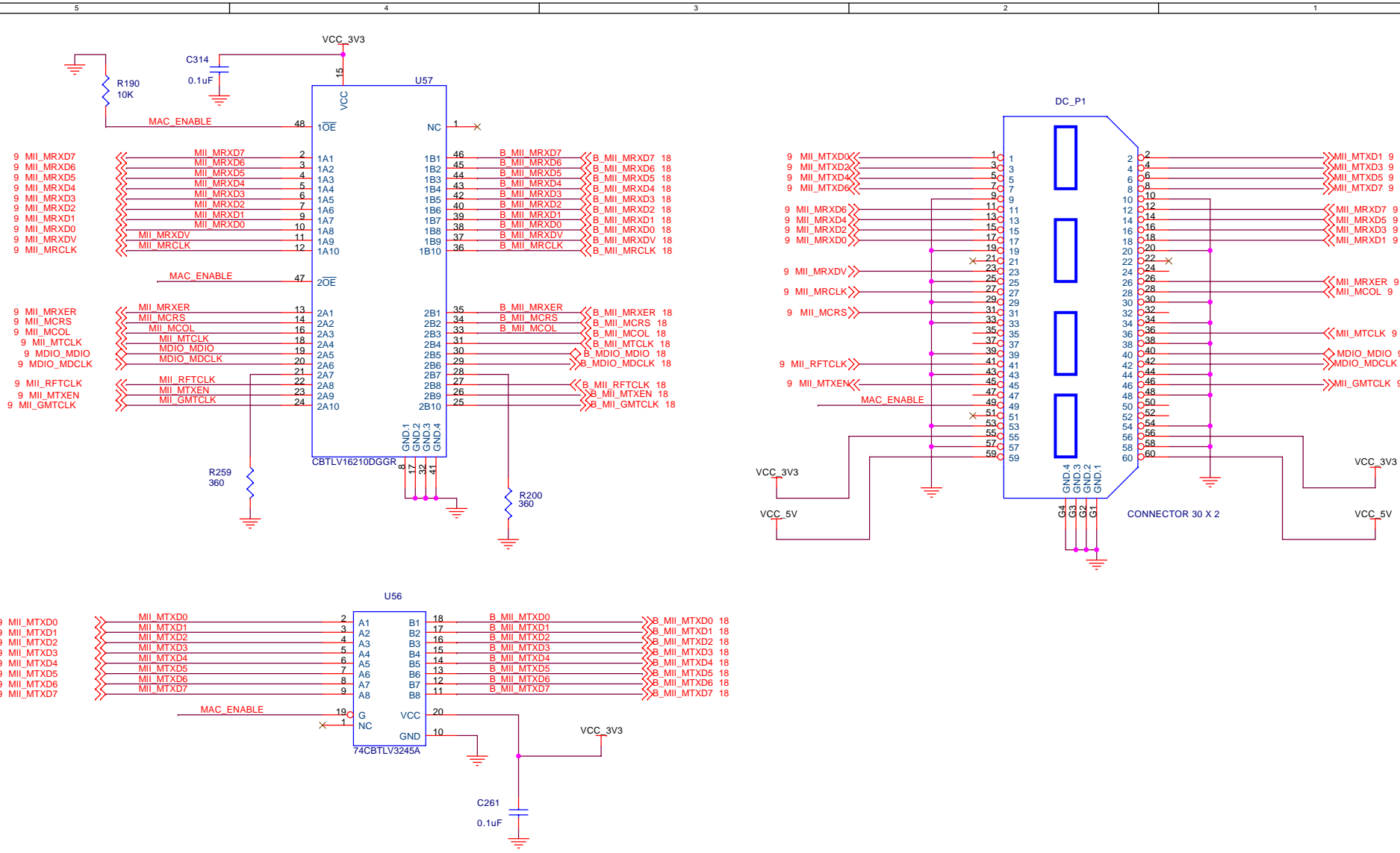


CE DON'T CARE DEVICE

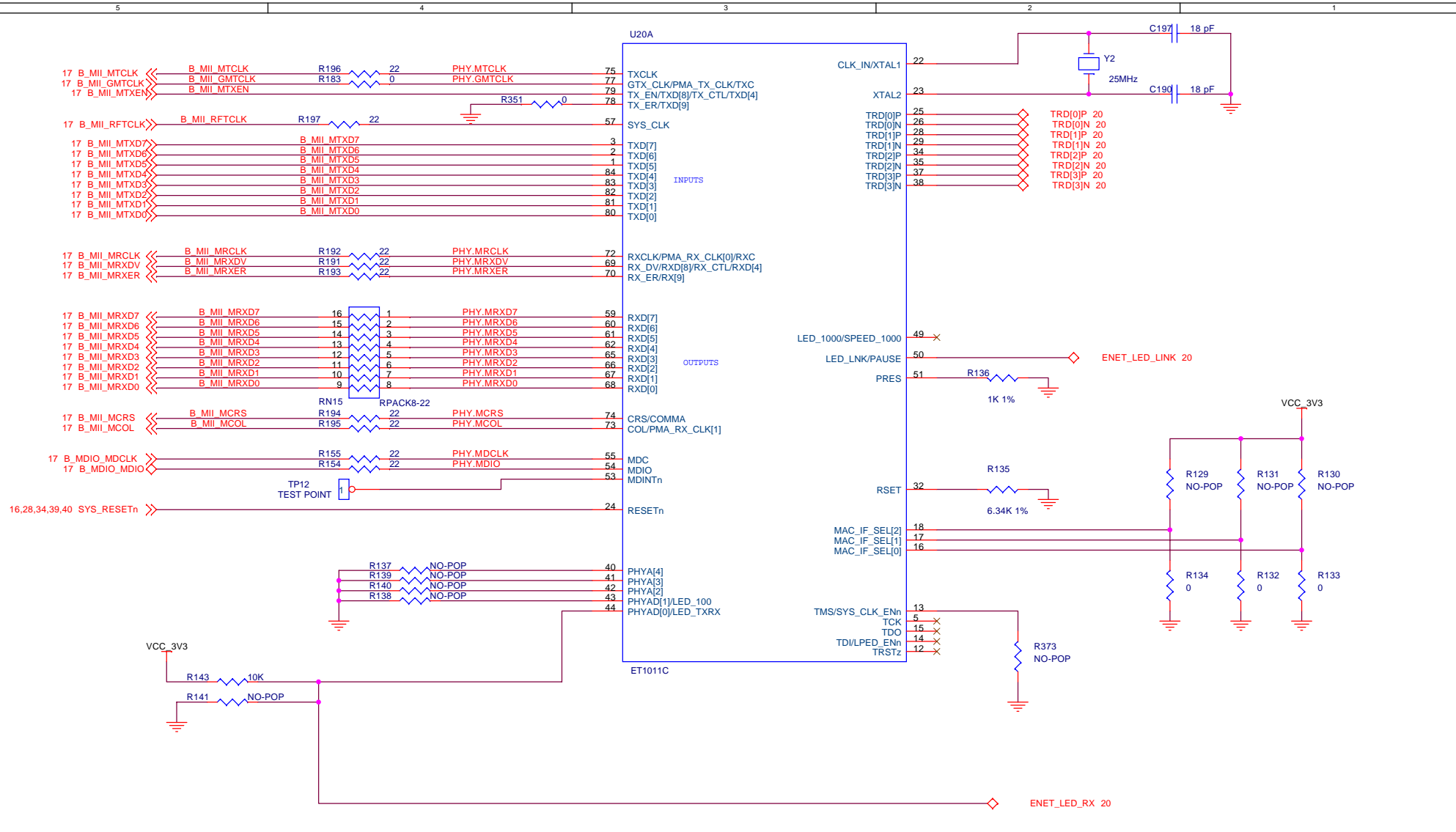
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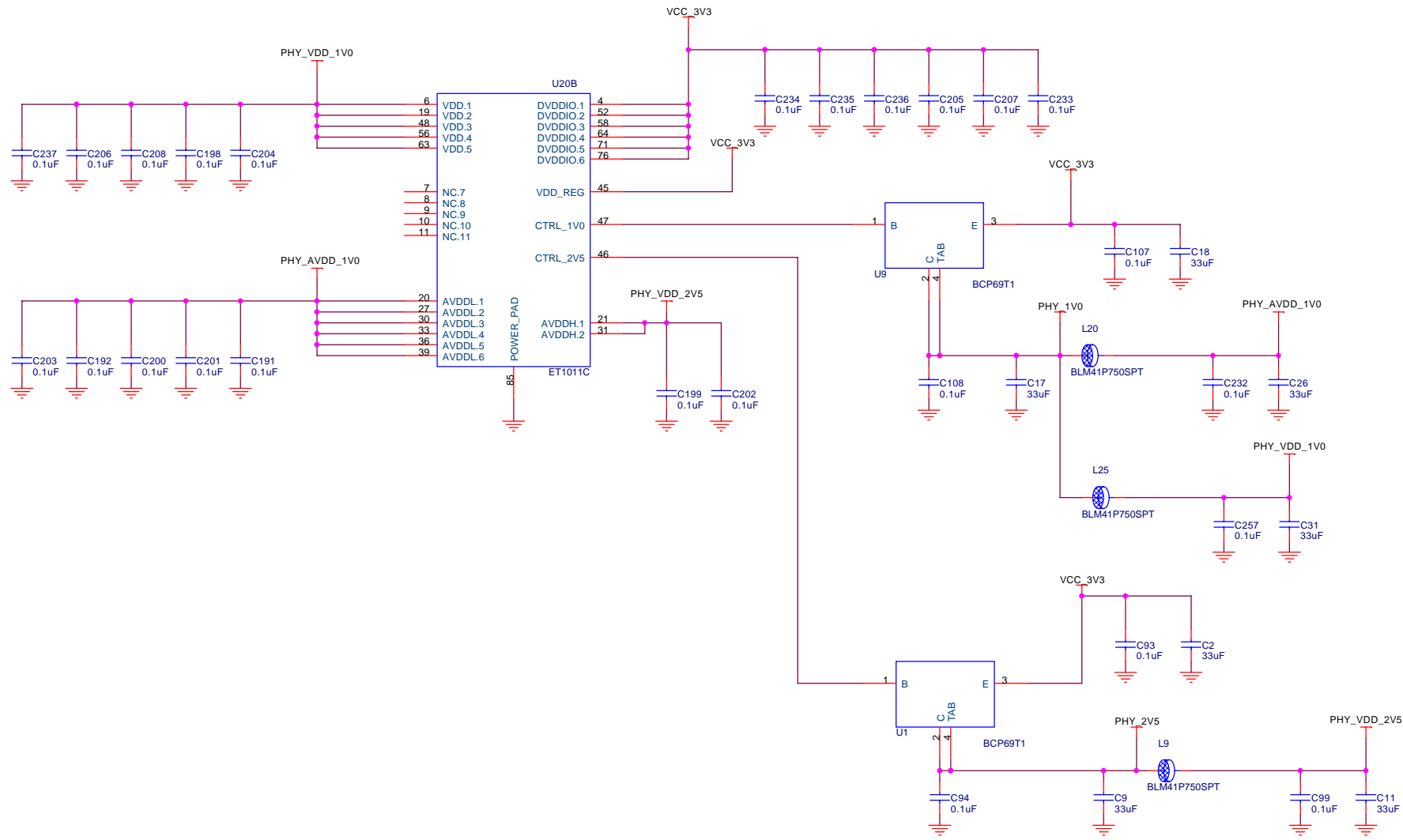
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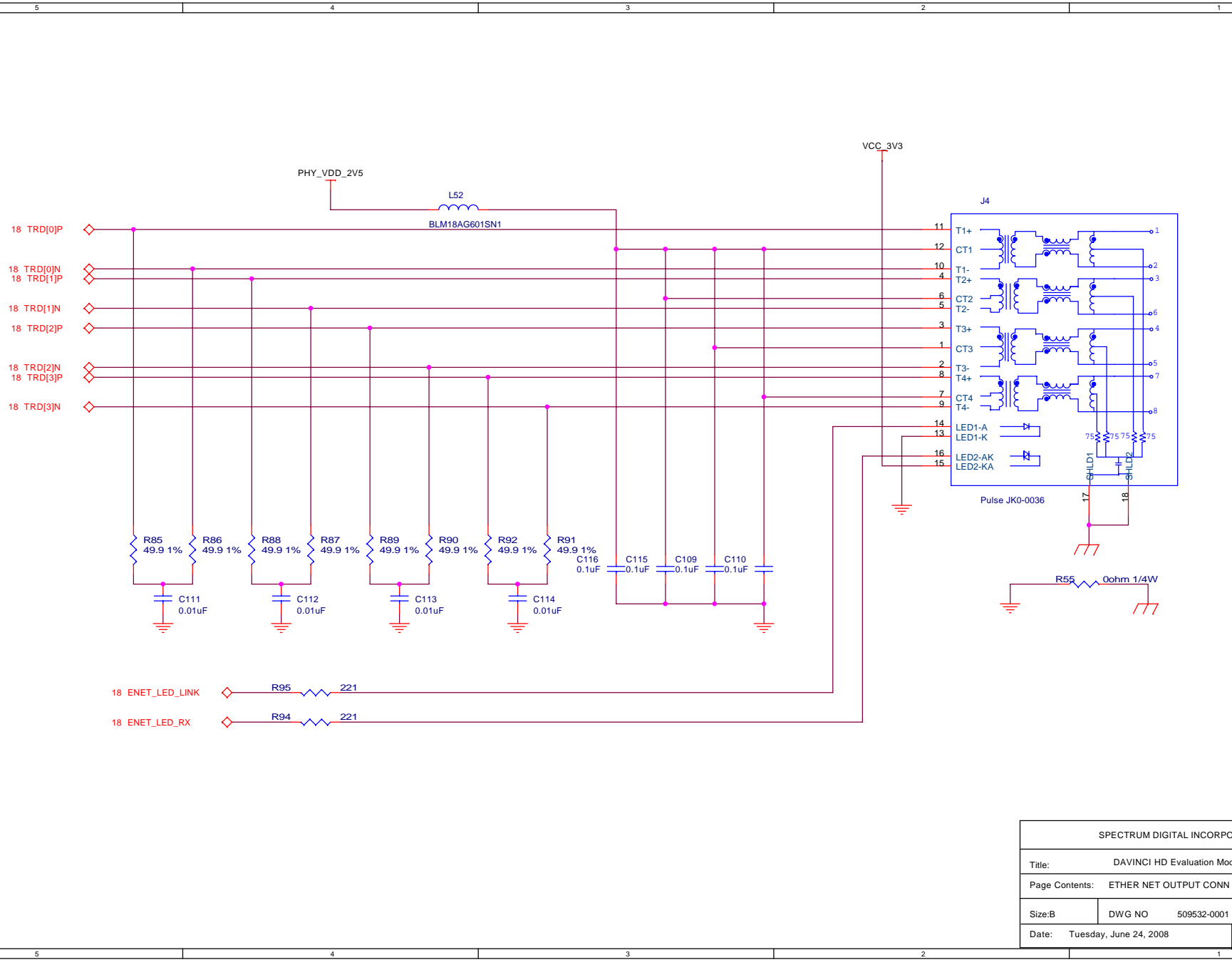
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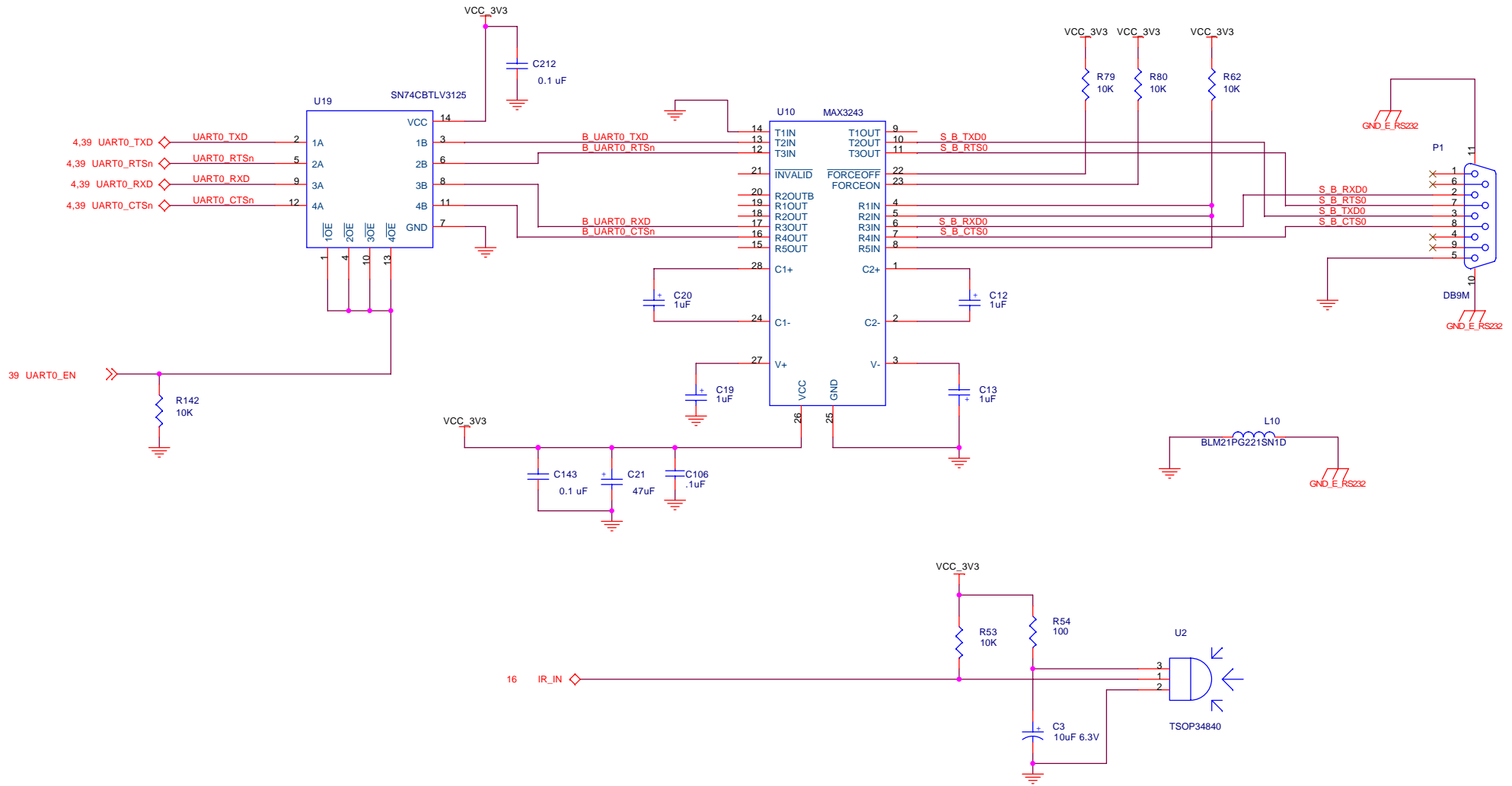
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Page Contents: ETHERNET INTERFACE			
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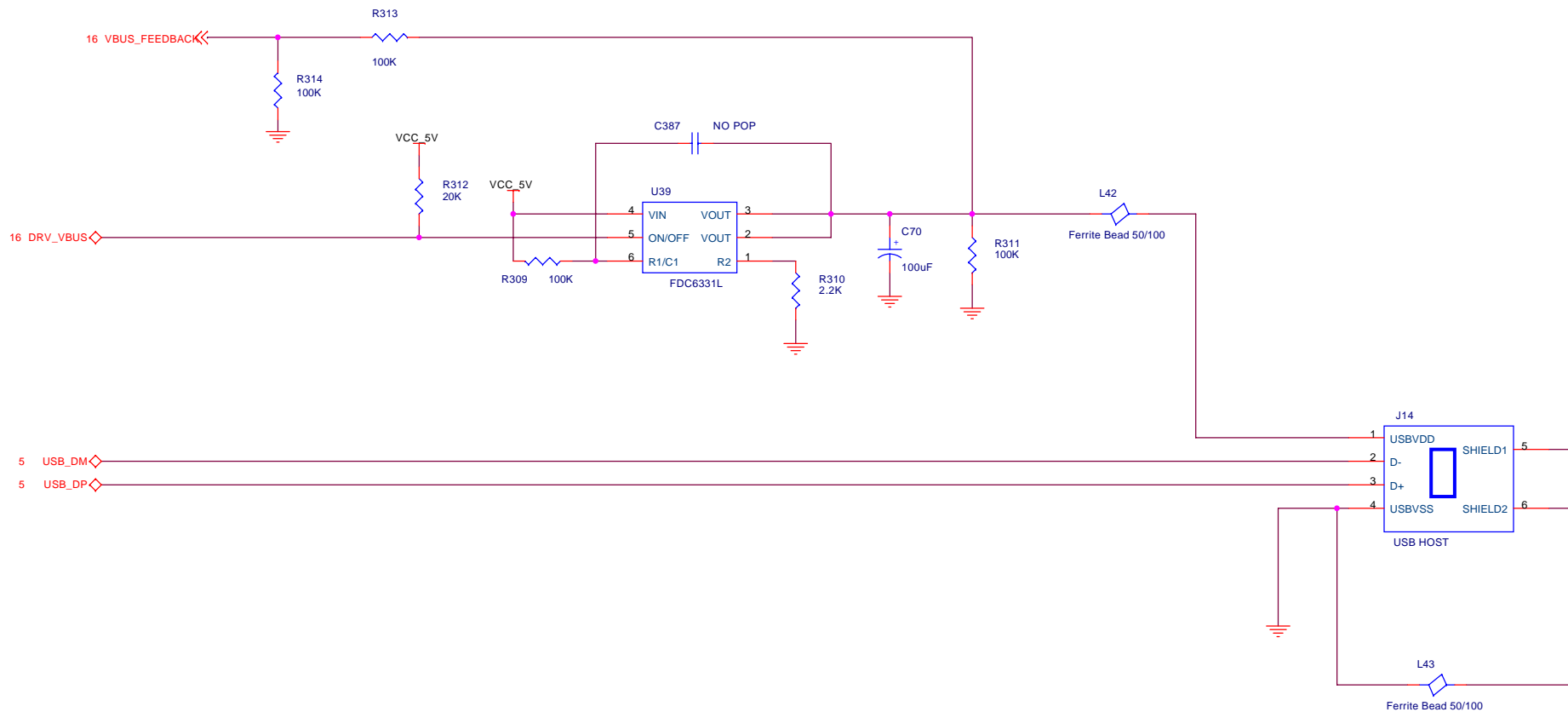
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Page Contents: ETHERNET - POWER			
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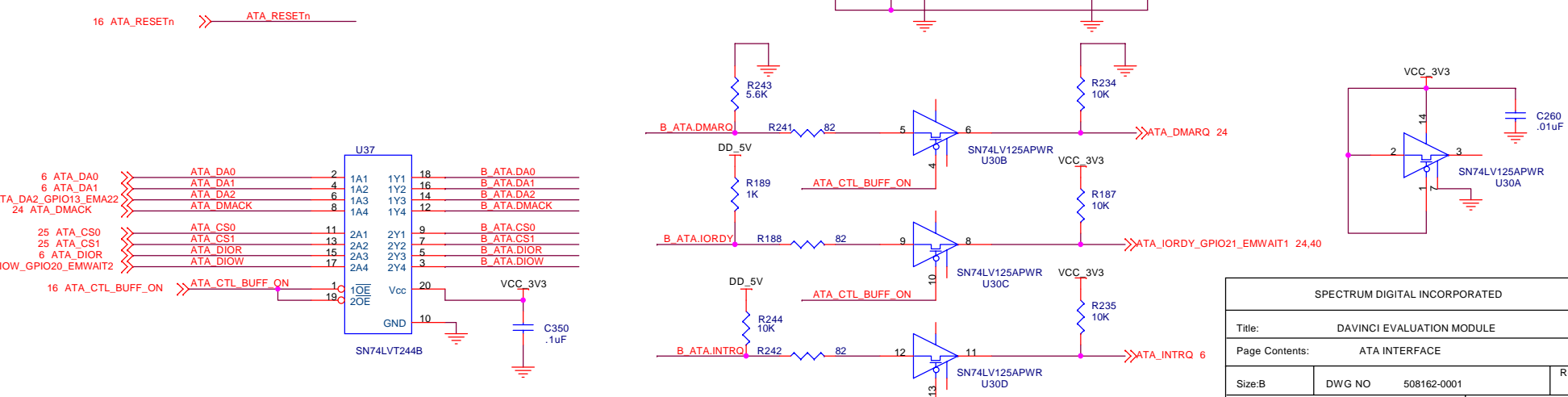
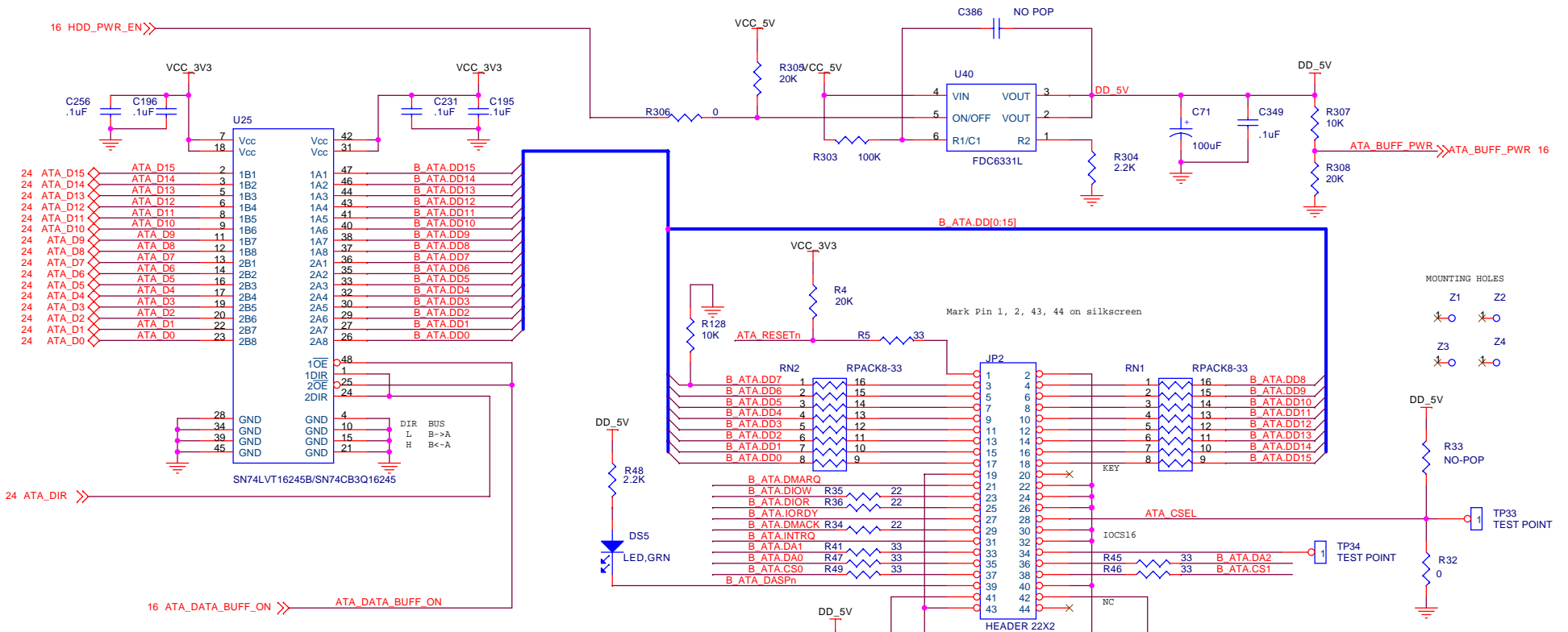
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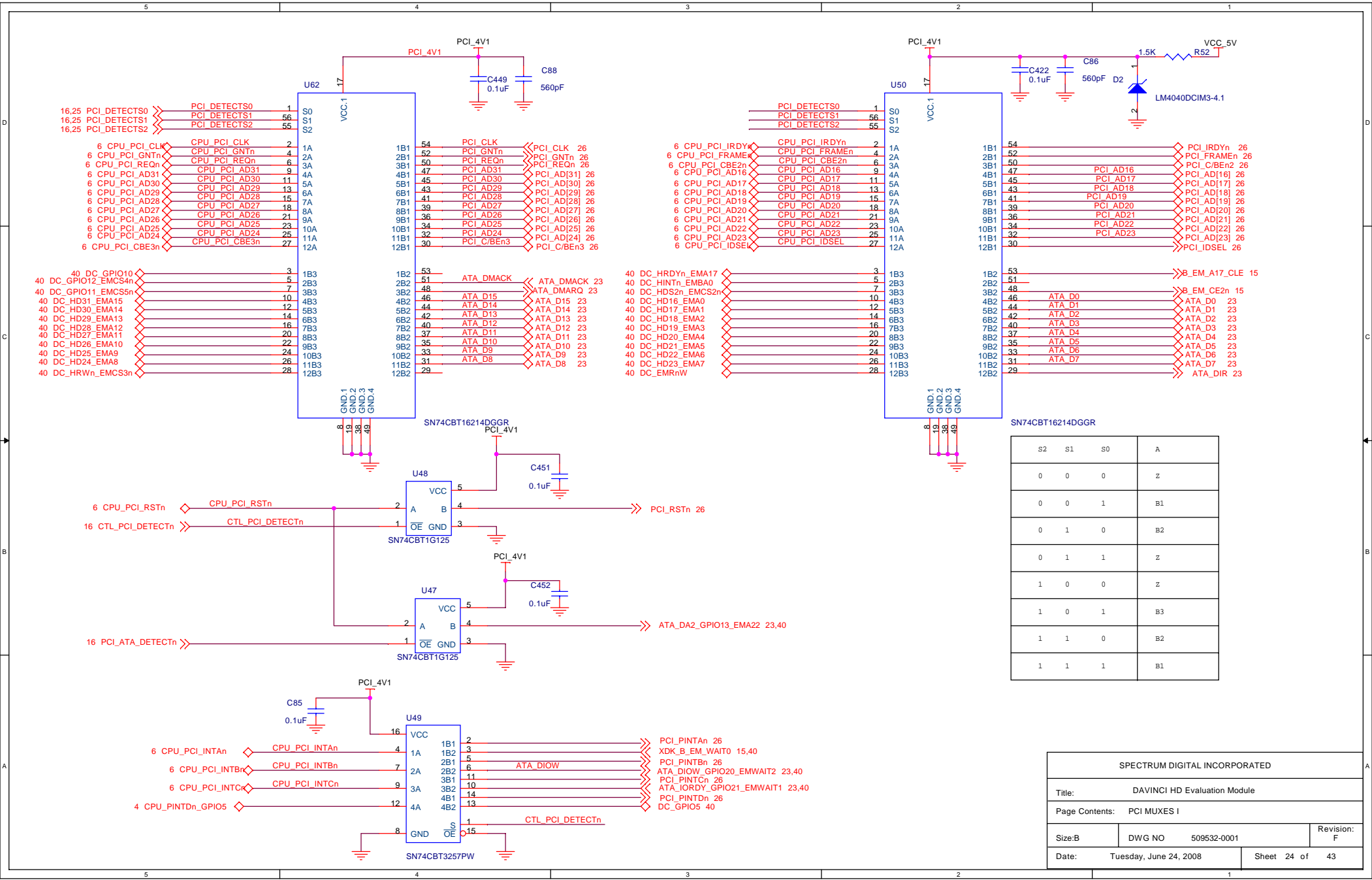
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Page Contents: UART0 RS232 / UART2 IR RECEIVER			
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TEXAS INSTRUMENTS INCORPORATED			
Title: DAVINCI HD Evaluation Module			
Page Contents: DAVINCI-HD USBII OUTPUT			
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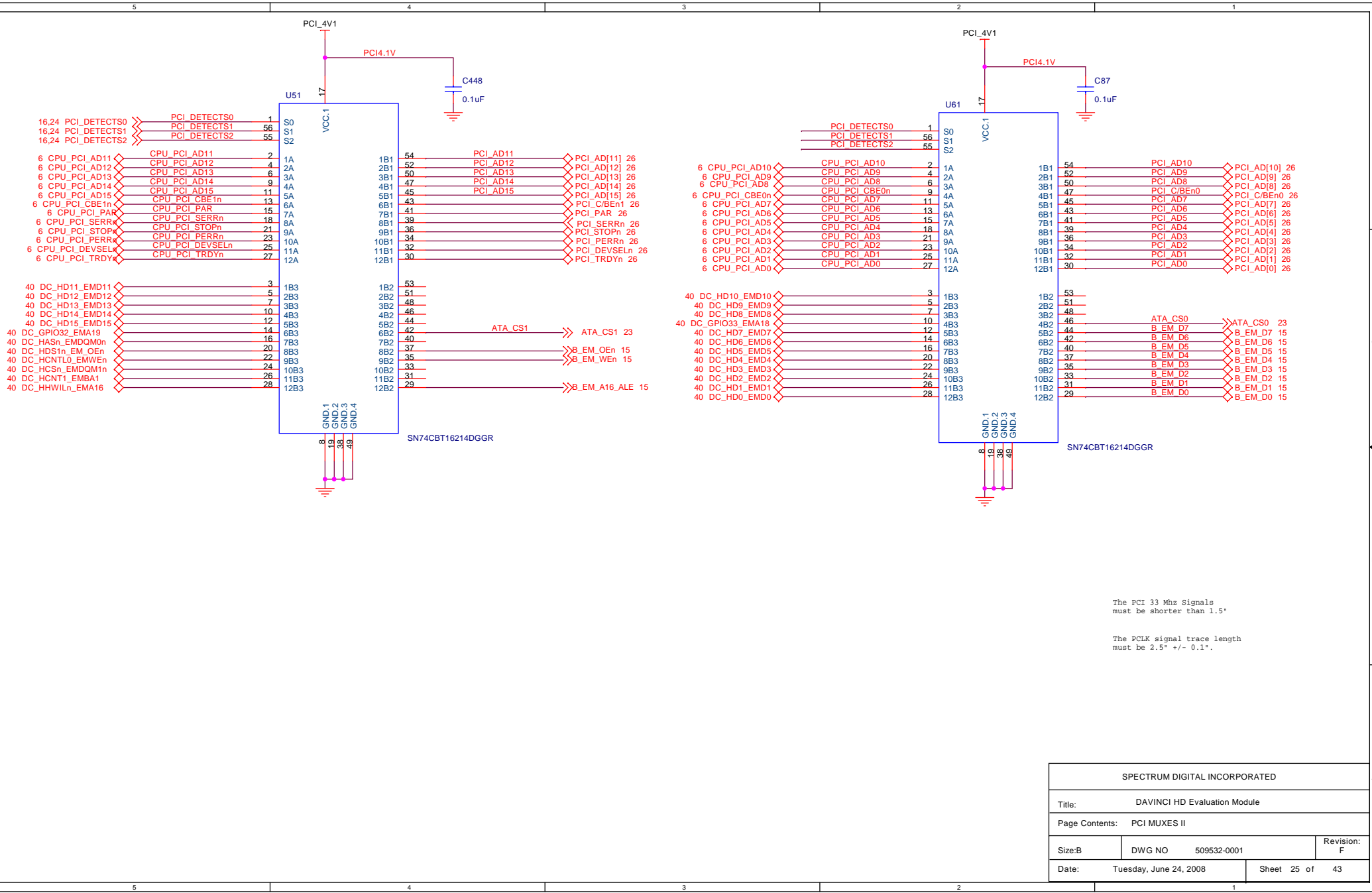


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Page Contents: ATA INTERFACE			
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S2	S1	S0	A
0	0	0	Z
0	0	1	B1
0	1	0	B2
0	1	1	Z
1	0	0	Z
1	0	1	B3
1	1	0	B2
1	1	1	B1

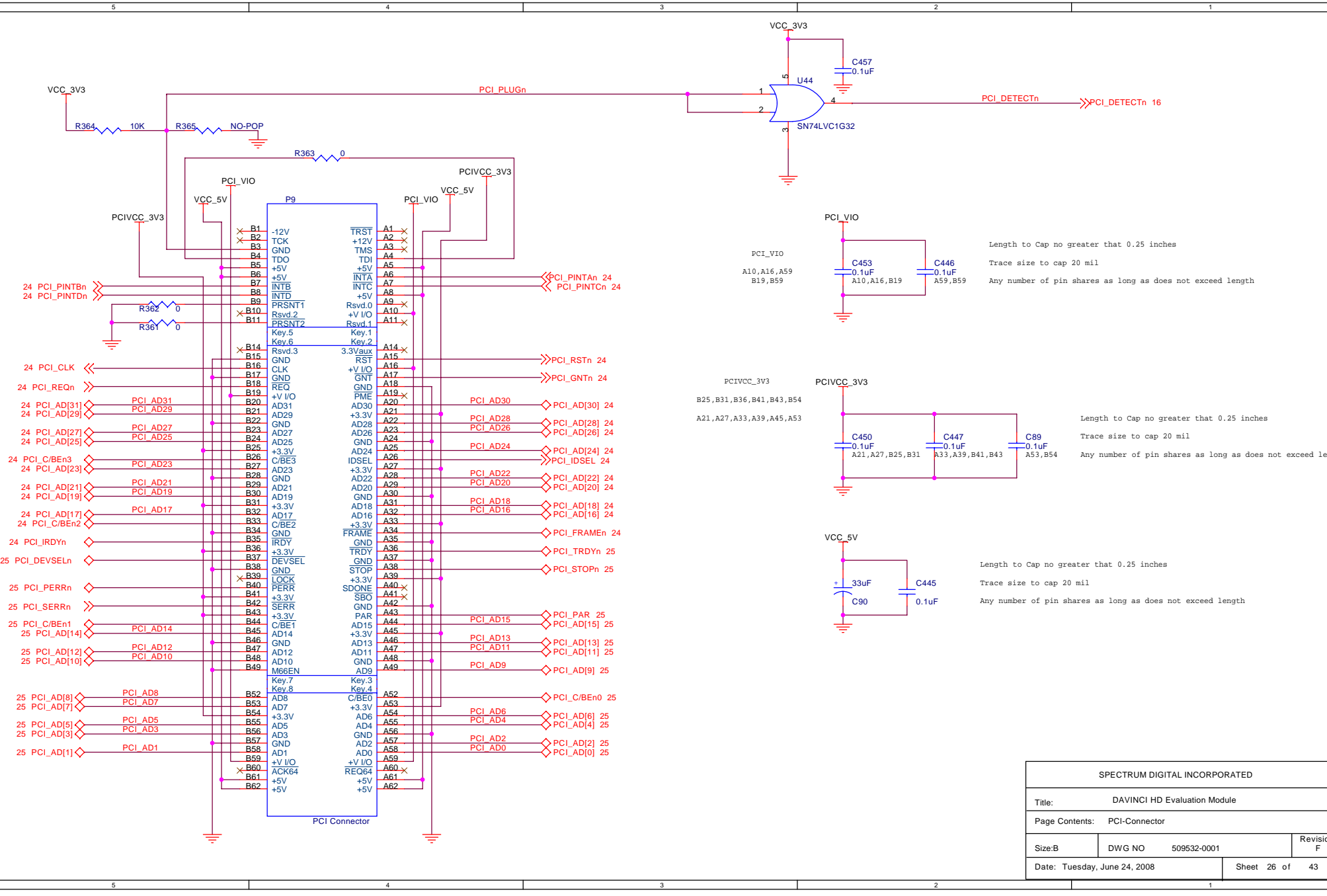
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Title: DAVINCI HD Evaluation Module			
Page Contents: PCI MUXES 1			
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The PCI 33 Mhz Signals must be shorter than 1.5"

The PCLK signal trace length must be 2.5" +/- 0.1".

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Page Contents: PCI MUXES II			
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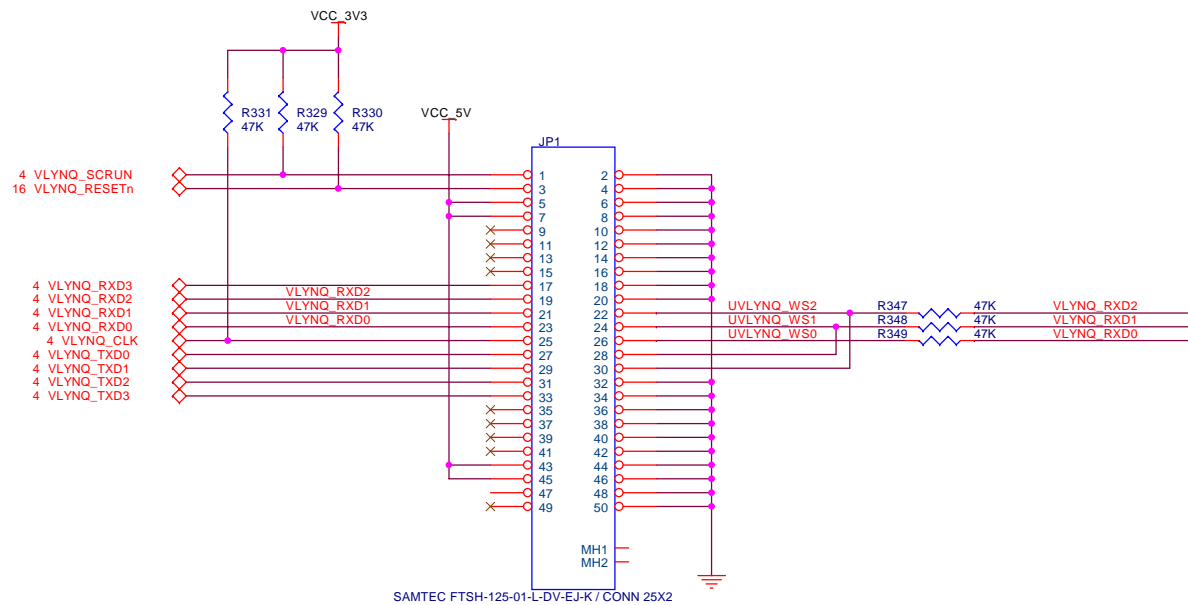


Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

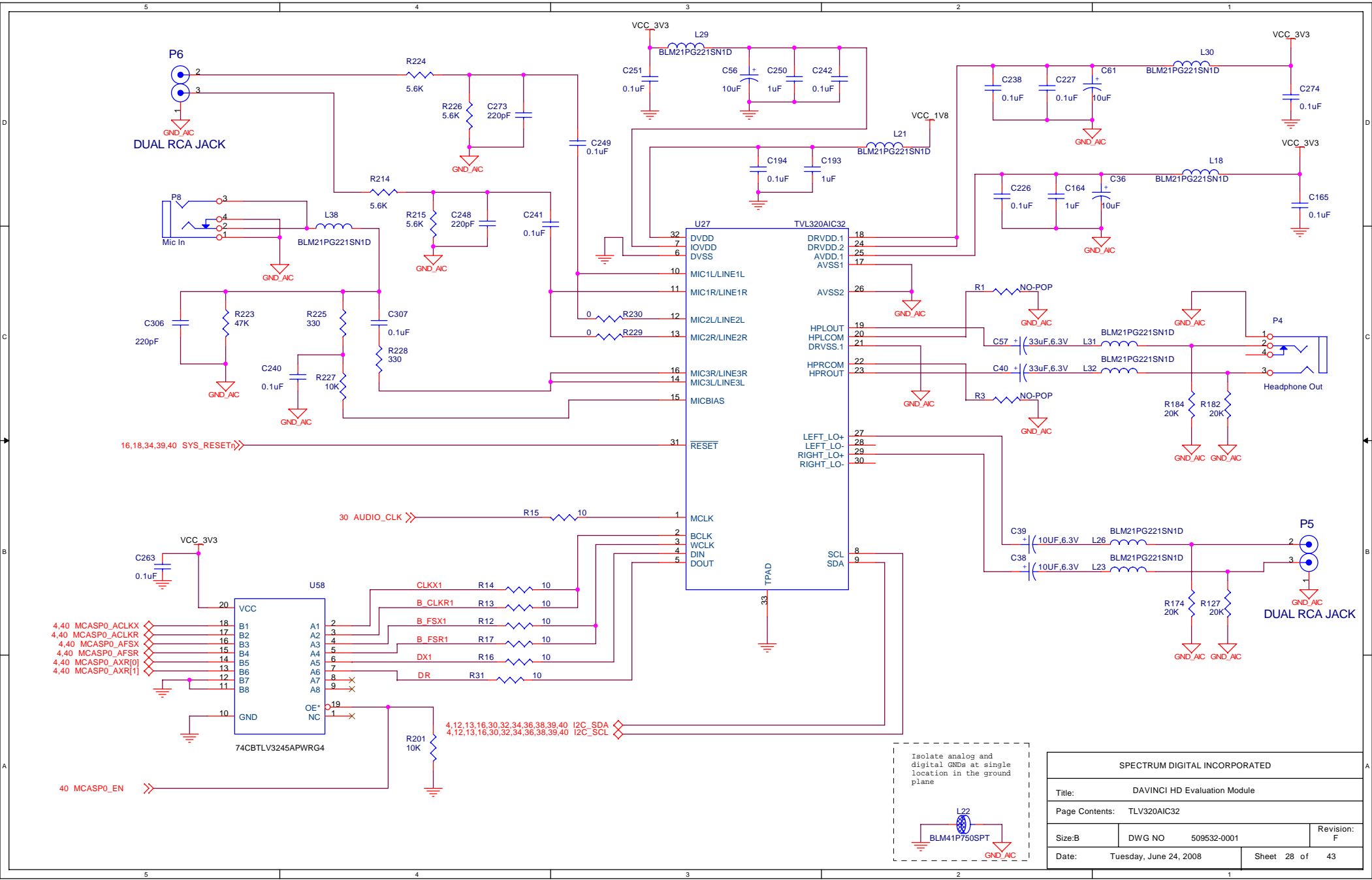
Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

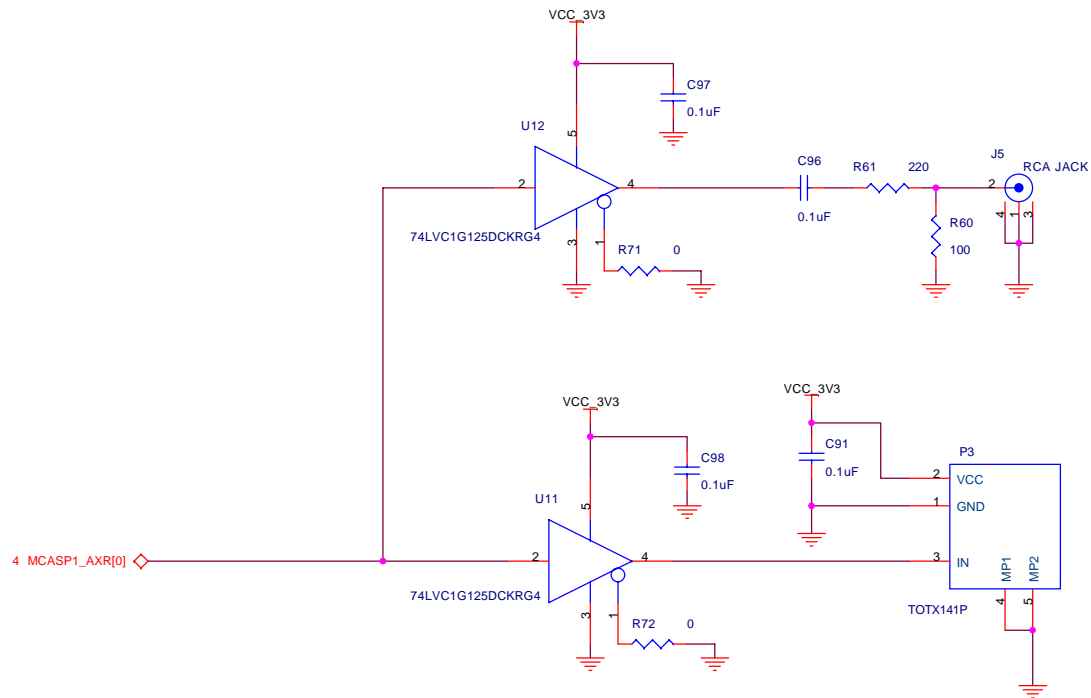
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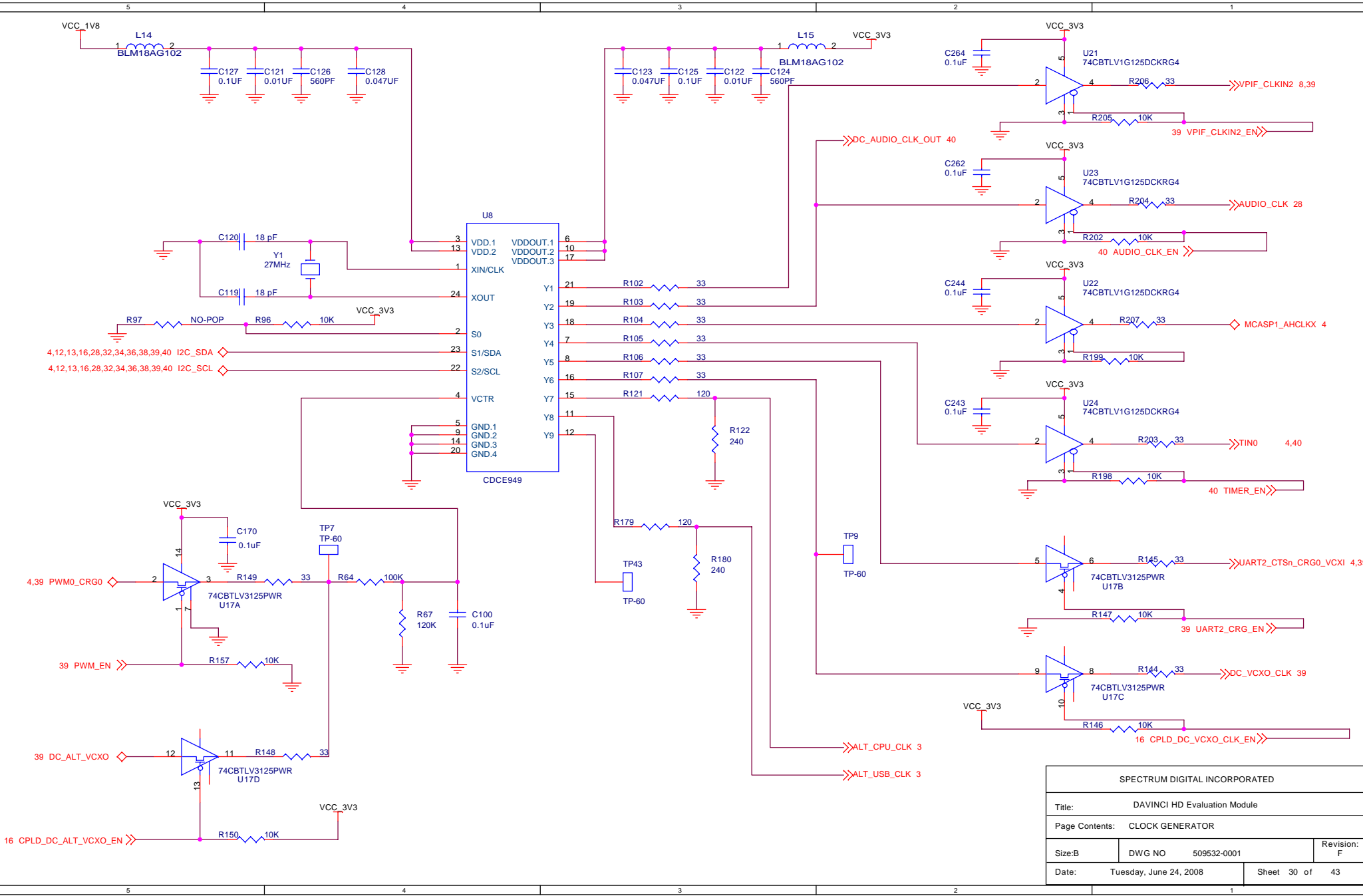
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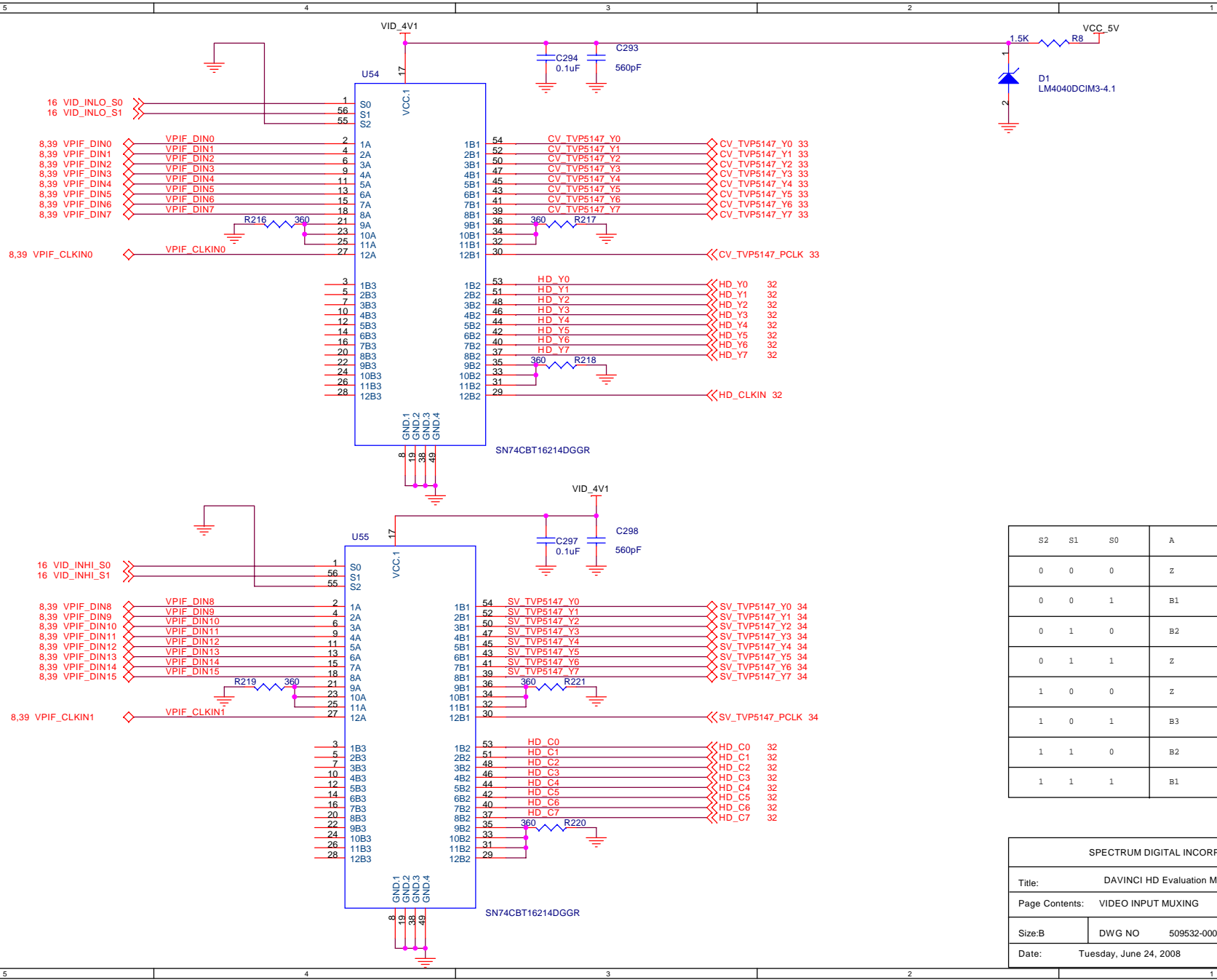
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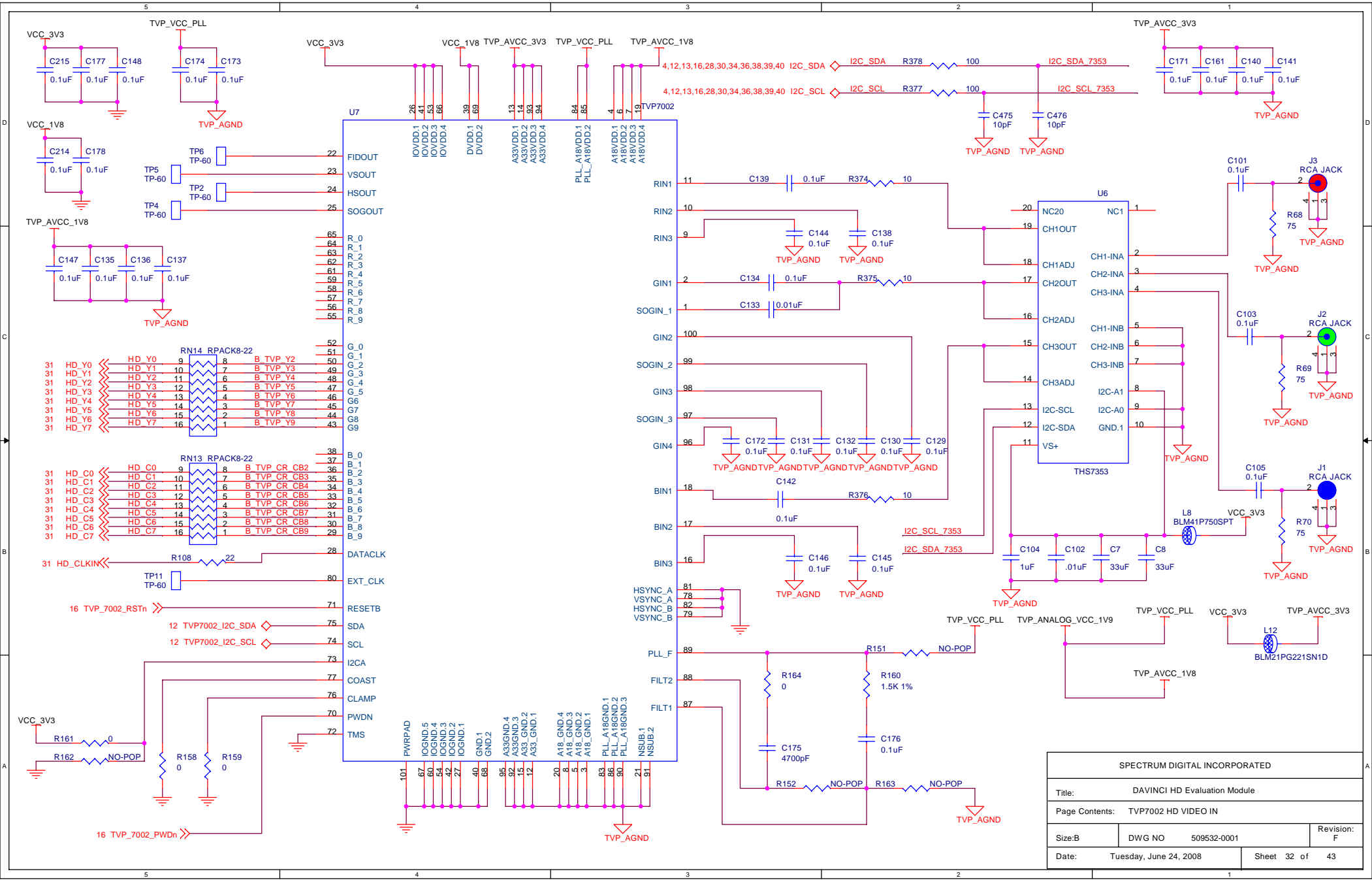


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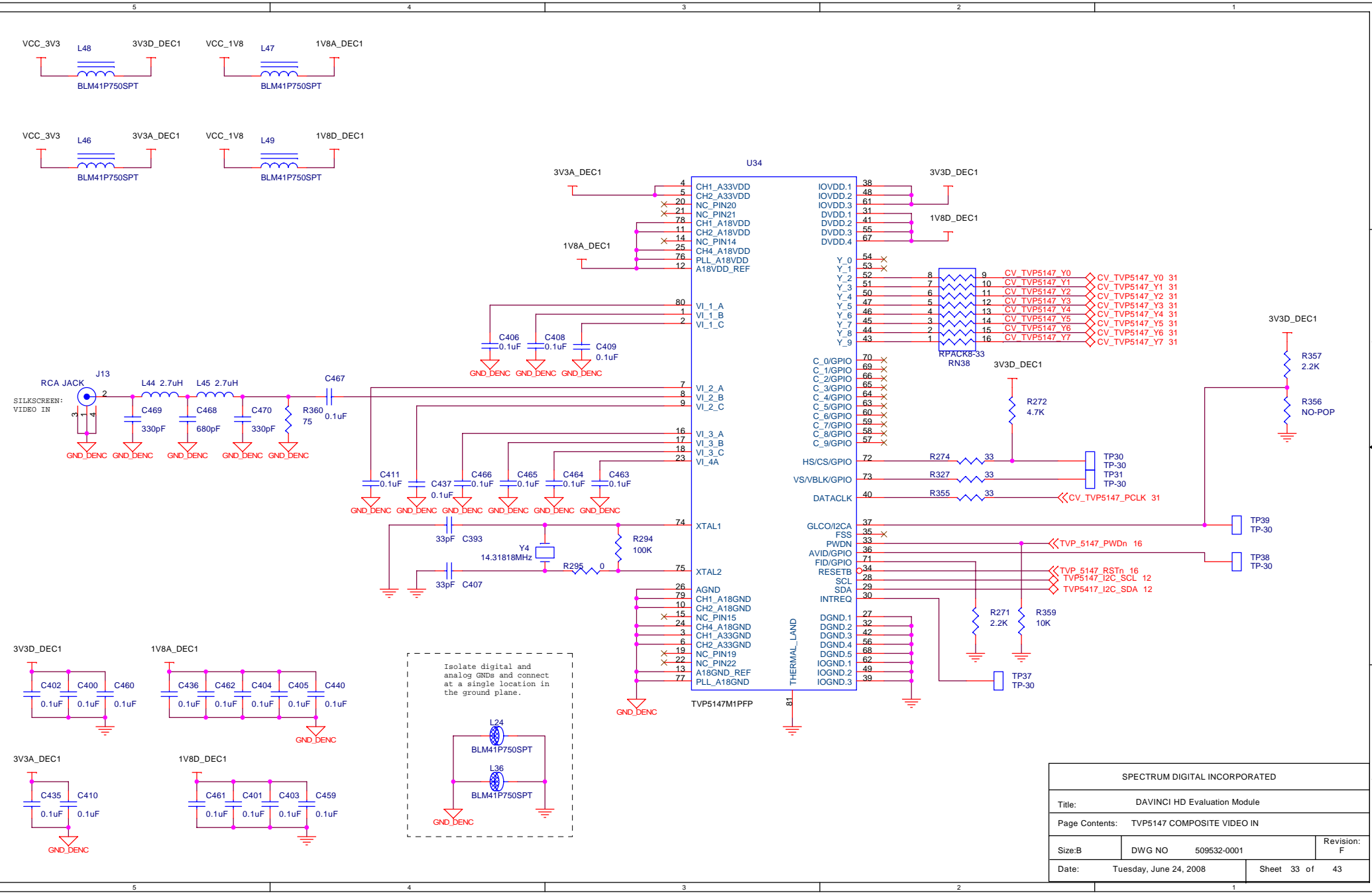


S2	S1	S0	A
0	0	0	Z
0	0	1	B1
0	1	0	B2
0	1	1	Z
1	0	0	Z
1	0	1	B3
1	1	0	B2
1	1	1	B1

SPECTRUM DIGITAL INCORPORATED			
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Page Contents: VIDEO INPUT MUXING			
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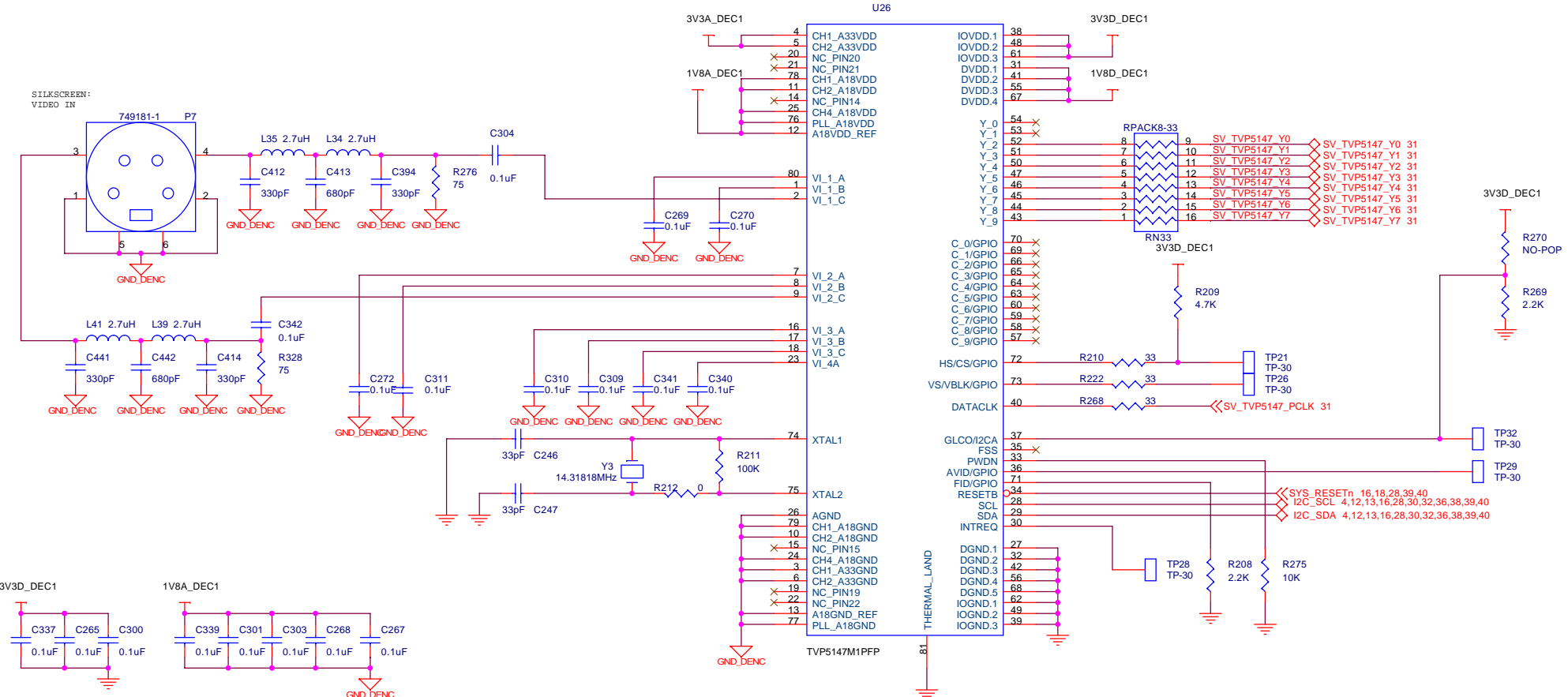


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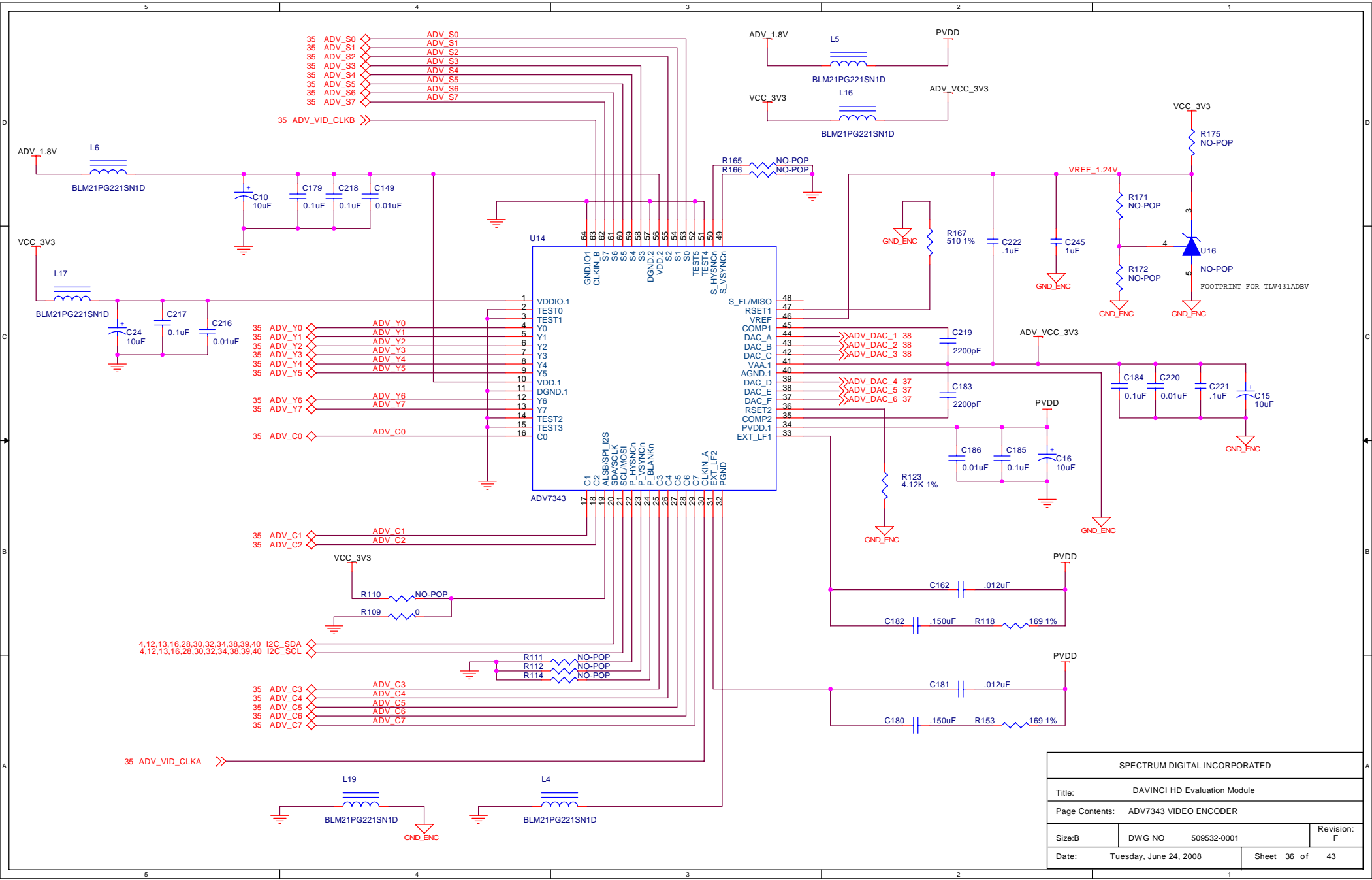


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Size: B	DWG NO	509532-0001	Revision: F
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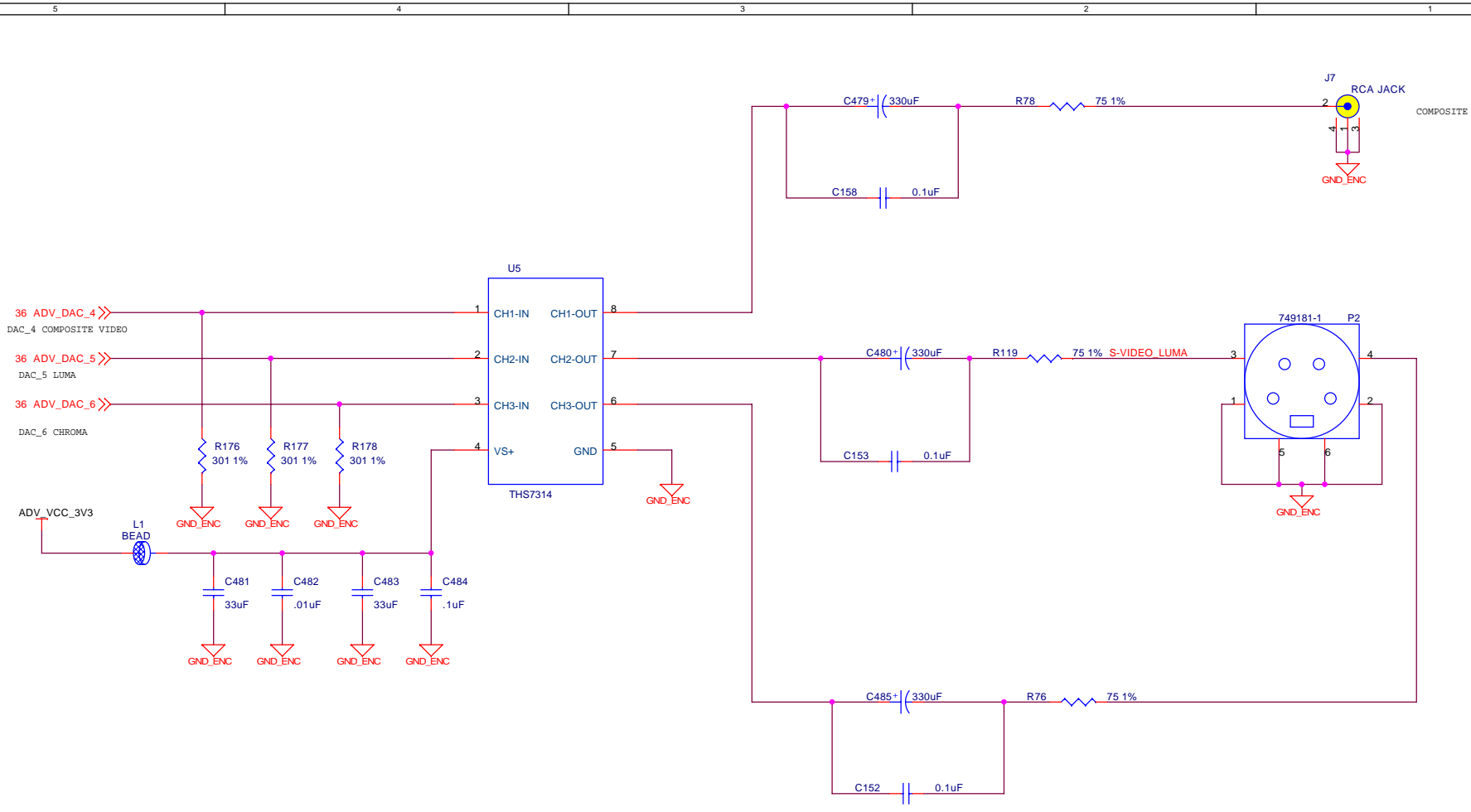
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VIDEO IN



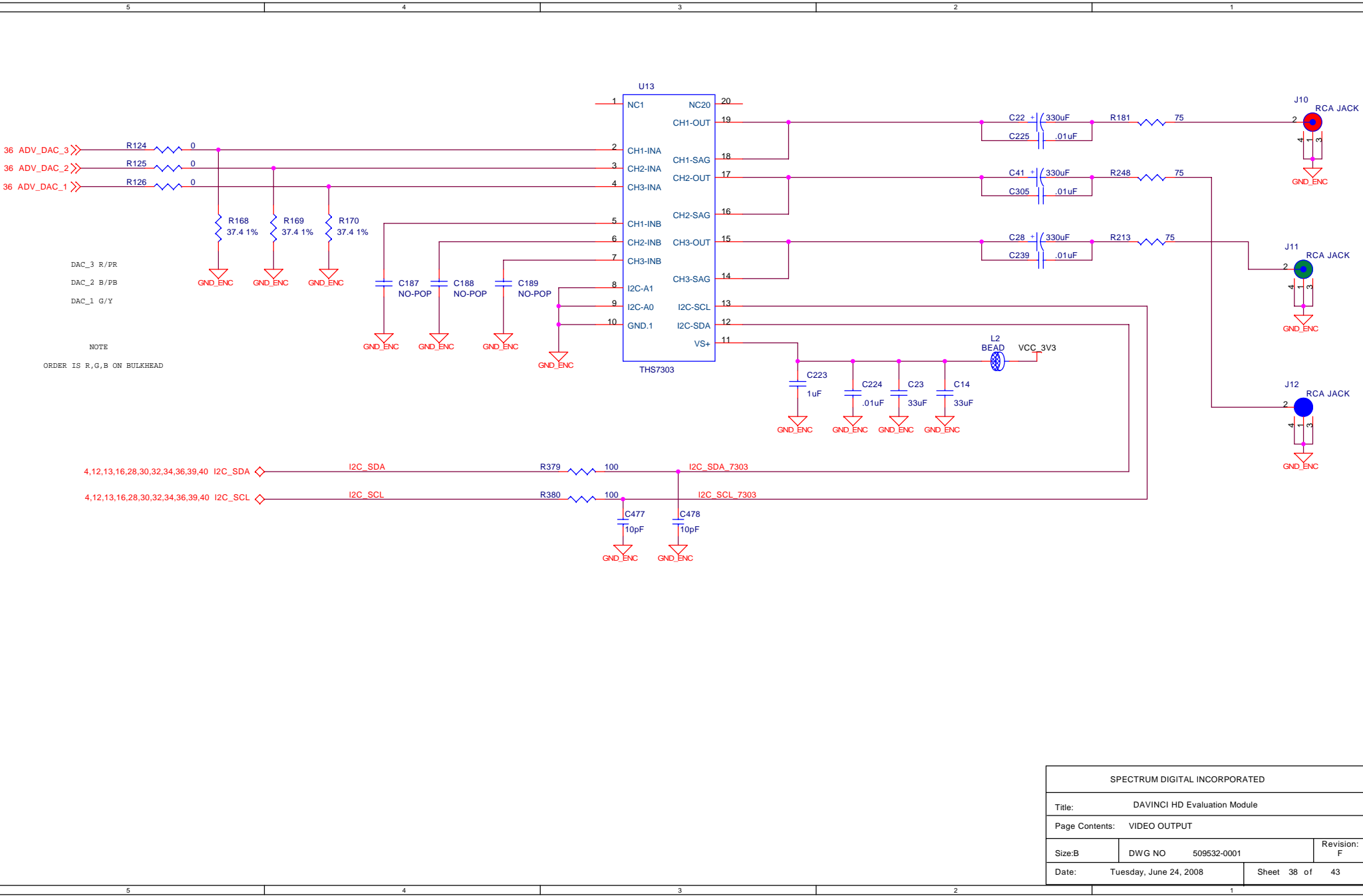
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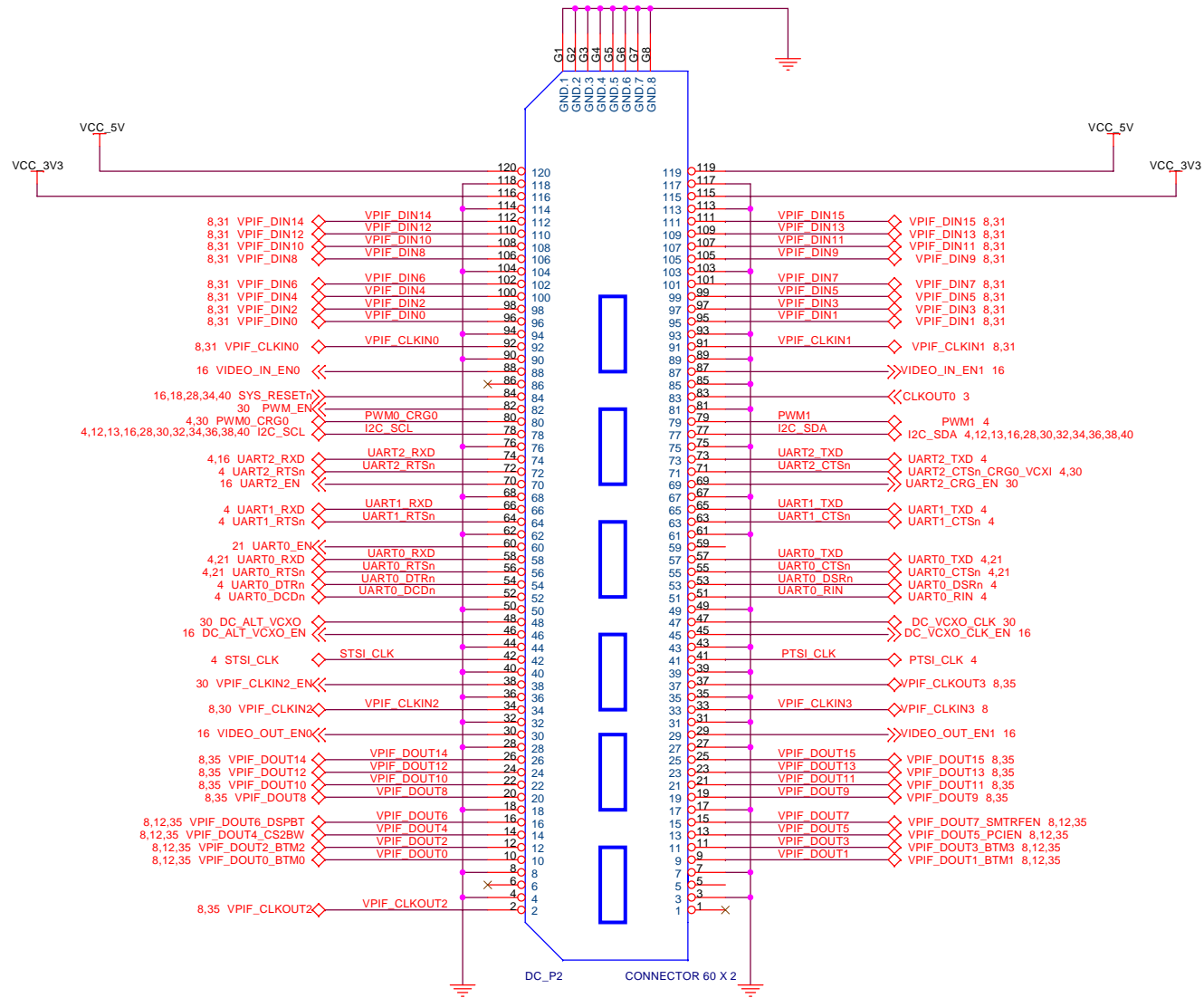
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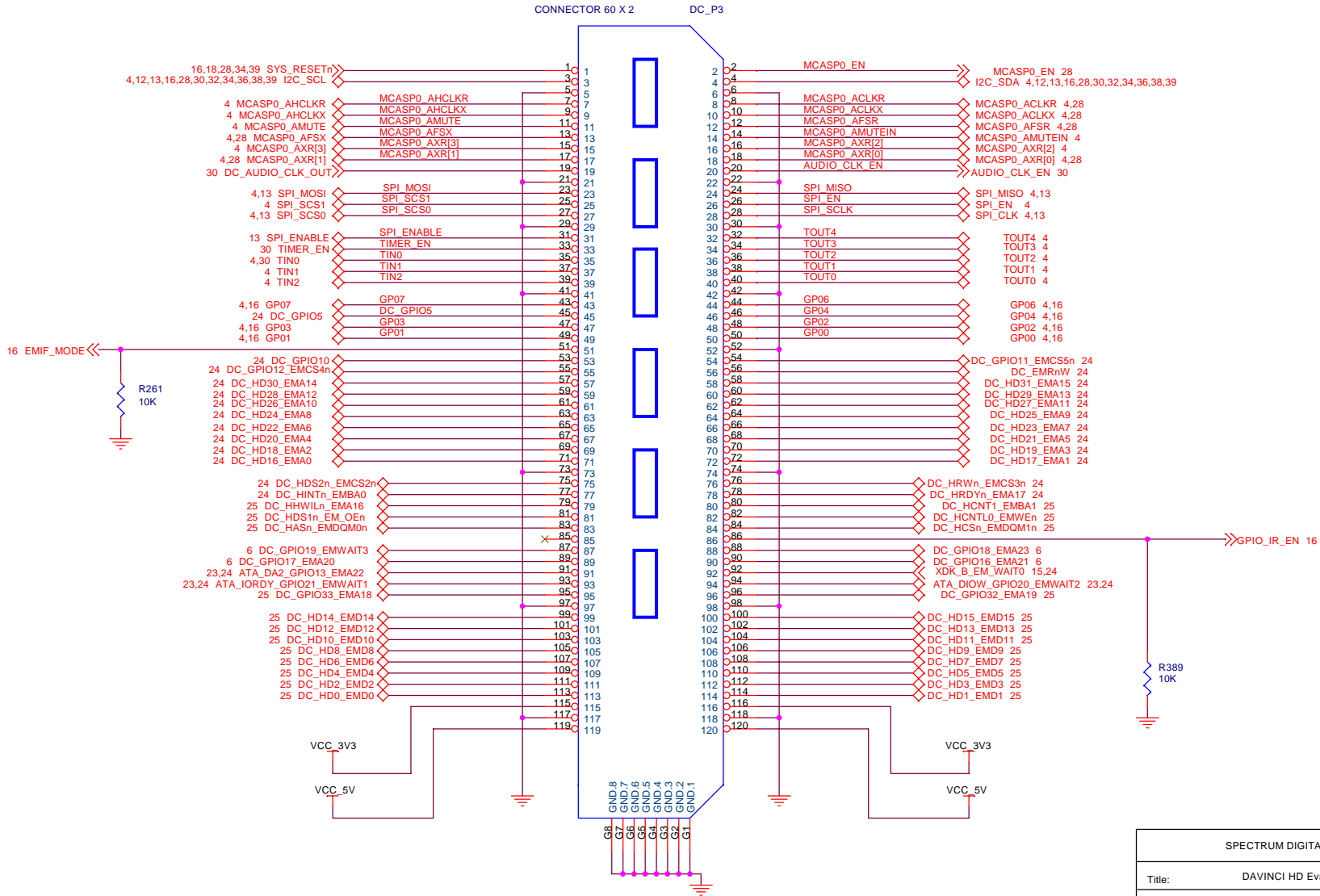
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Size: B	DWG NO	509532-0001	Revision: F
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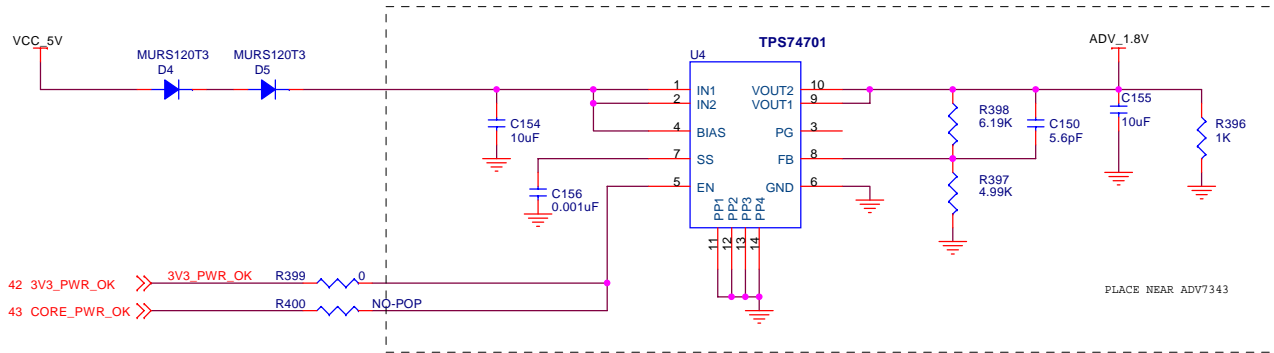
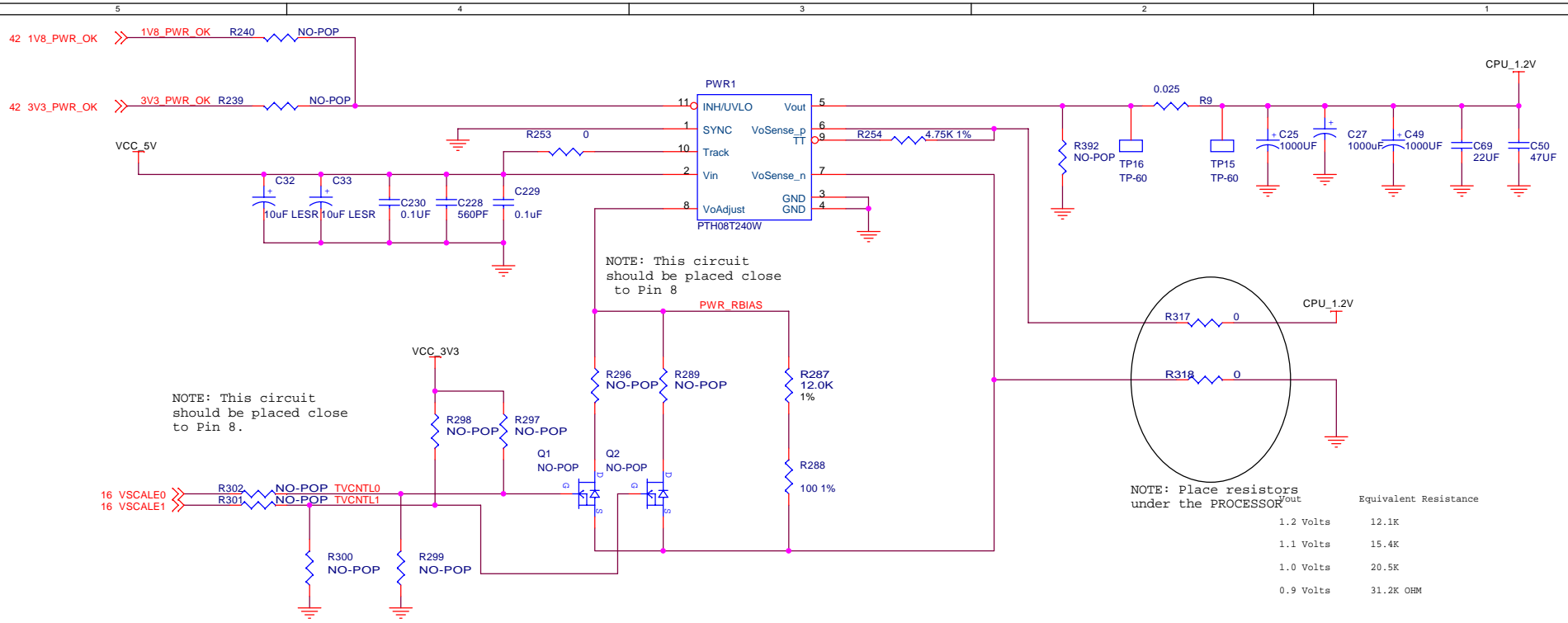
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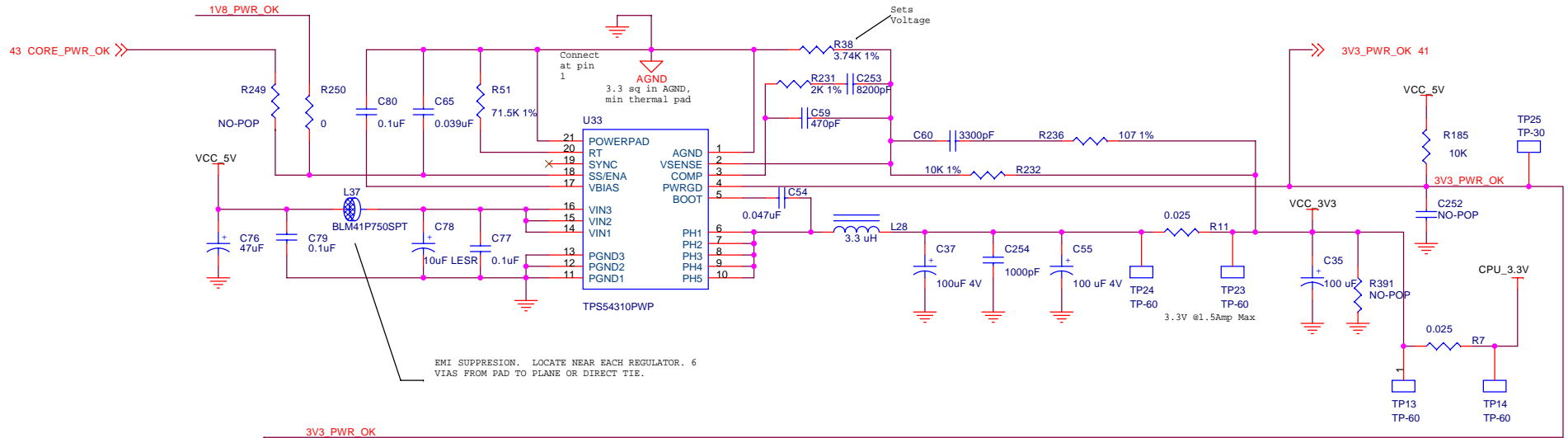
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Size: B	DWG NO	509532-0001	Revision: F
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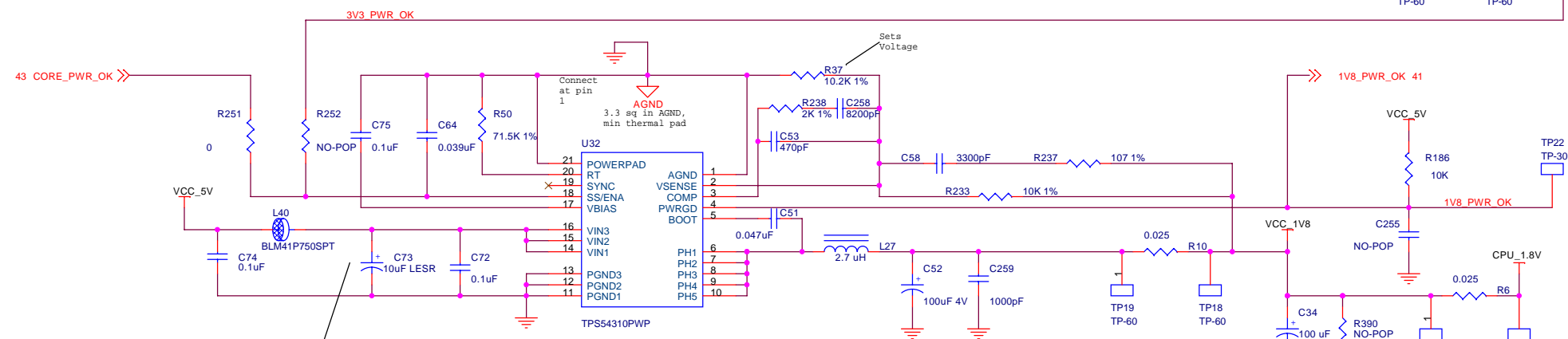
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Page Contents: I/O DAUGHTER CARD CONNECTOR			
Size: B	DWG NO	509532-0001	Revision: F
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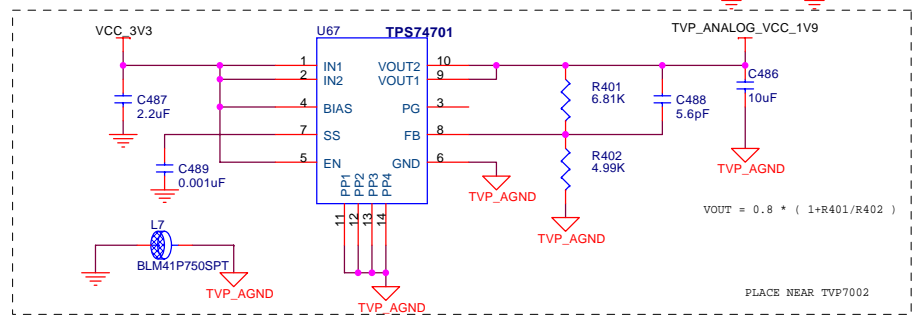
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Title: DAVINCI HD Evaluation Module			
Page Contents: DSP CORE POWER			
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EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.



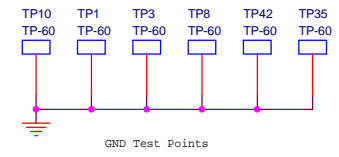
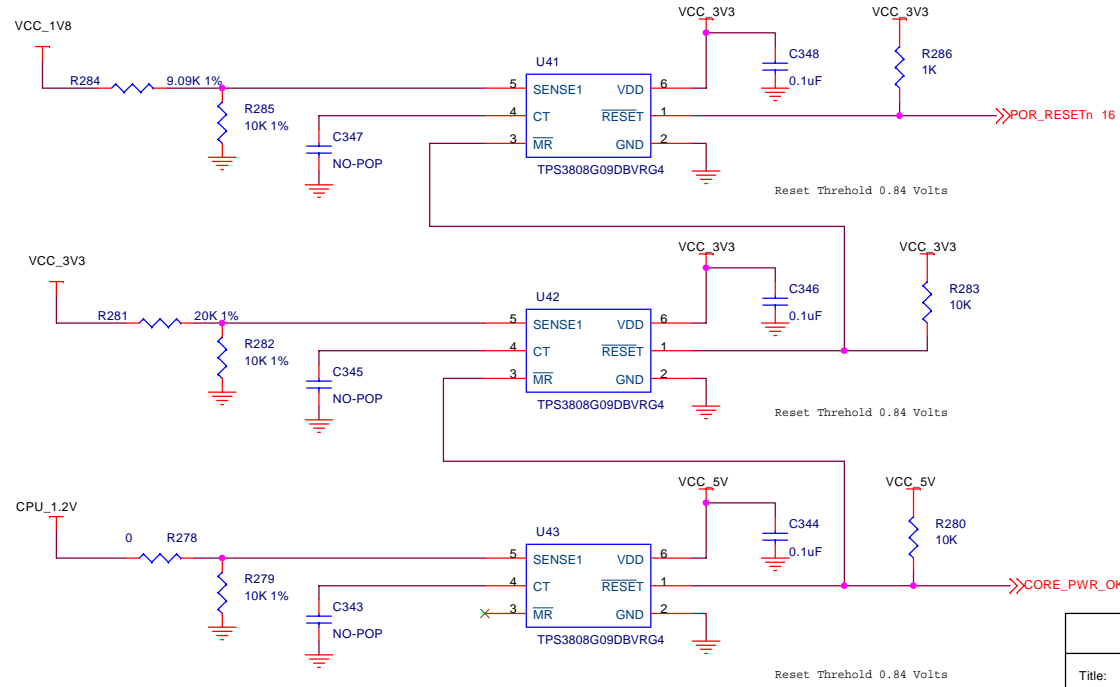
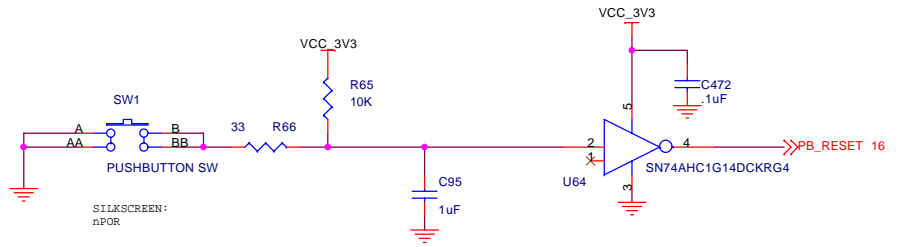
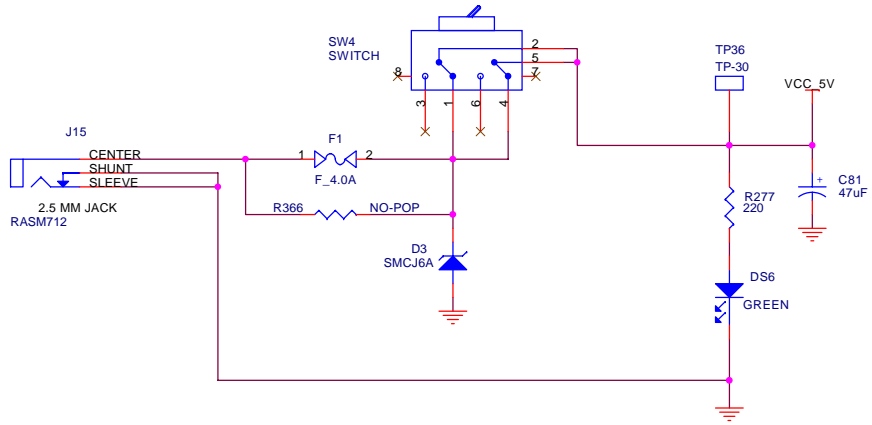
EMI SUPPRESSION. LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.



$$VOUT = 0.8 * (1 + R401/R402)$$

PLACE NEAR TVP7002

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