

NOTES, UNLESS OTHERWISE SPECIFIED:

- 1. RESISTANCE VALUES IN OHMS.
- 2. CAPACITANCE VALUES IN MICROFARADS.
- 3. REFERENCE DESIGNATORS USED:
- 4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic for layout	11/15/2010	RRP
B	Added SDRAM/SPI FLASH/General updates	2/15/2011	RRP

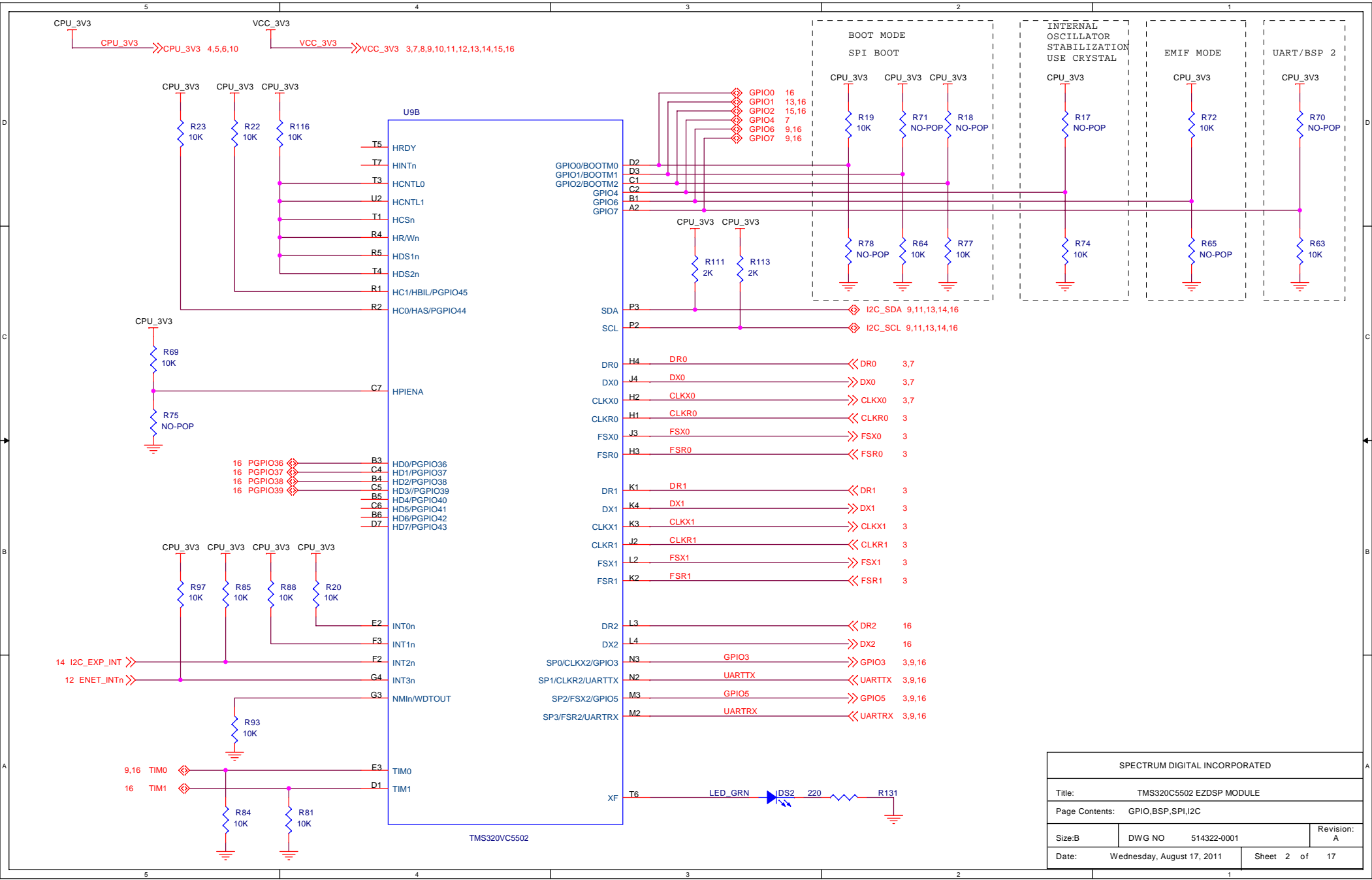
SCHEMATIC CONTENTS

- 01 - TITLE PAGE
- 02 - TMS320C5502 GPIO/BSP/SPI/I2C
- 03 - McBSP MUXES
- 04 - TMS320C5502 CLK/JTAG
- 05 - TMS320C5502 EMIF
- 06 - TMS320C5502 POWER
- 07 - SPI FLASH
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- 09 - CC BOARD INTERFACE
- 10 - POWER SUPPLIES
- 11 - AUDIO CODEC
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- 13 - LCD INTERFACE
- 14 - USER LEDS/SWITCHES
- 15 - FINGERPRINT INTERFACE
- 16 - EXPANSION CONNECTOR
- 17 - XDS100-v2 INTERFACE

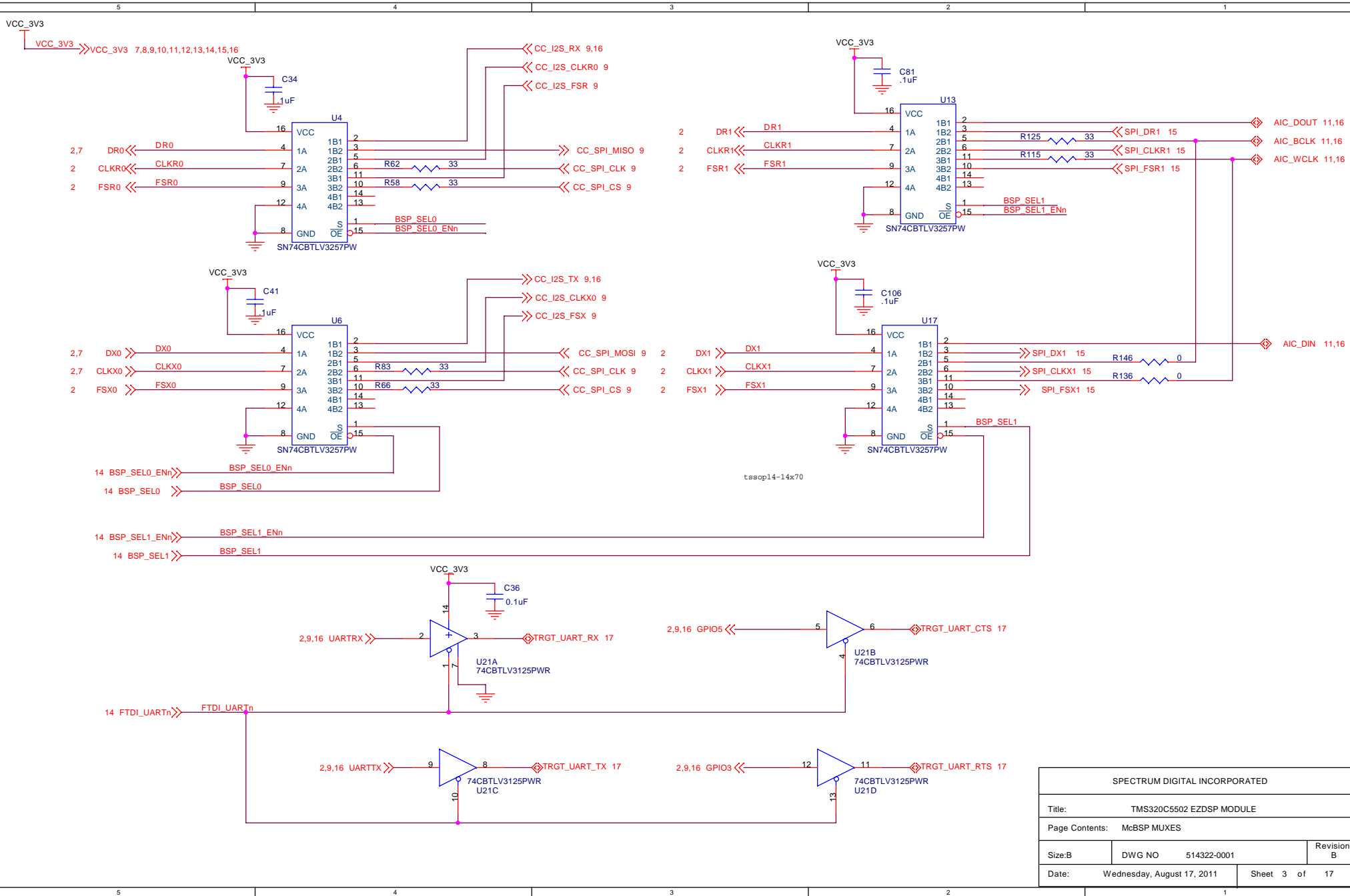
REVISION STATUS OF SHEETS

REV	SHEET	1	2	3	4	5	6	7	8	9	10	DATE	BY	DESCRIPTION
												11/15/2010	R.R.P.	DWN
												11/15/2010	T.W.K.	CHK
												11/15/2010	R.R.P.	ENGR
												11/15/2010	R.R.P.	ENGR-MGR
												11/15/2010	C.M.D.	QA
												11/15/2010	R.R.P.	MFG
												11/15/2010	R.R.P.	RLSE

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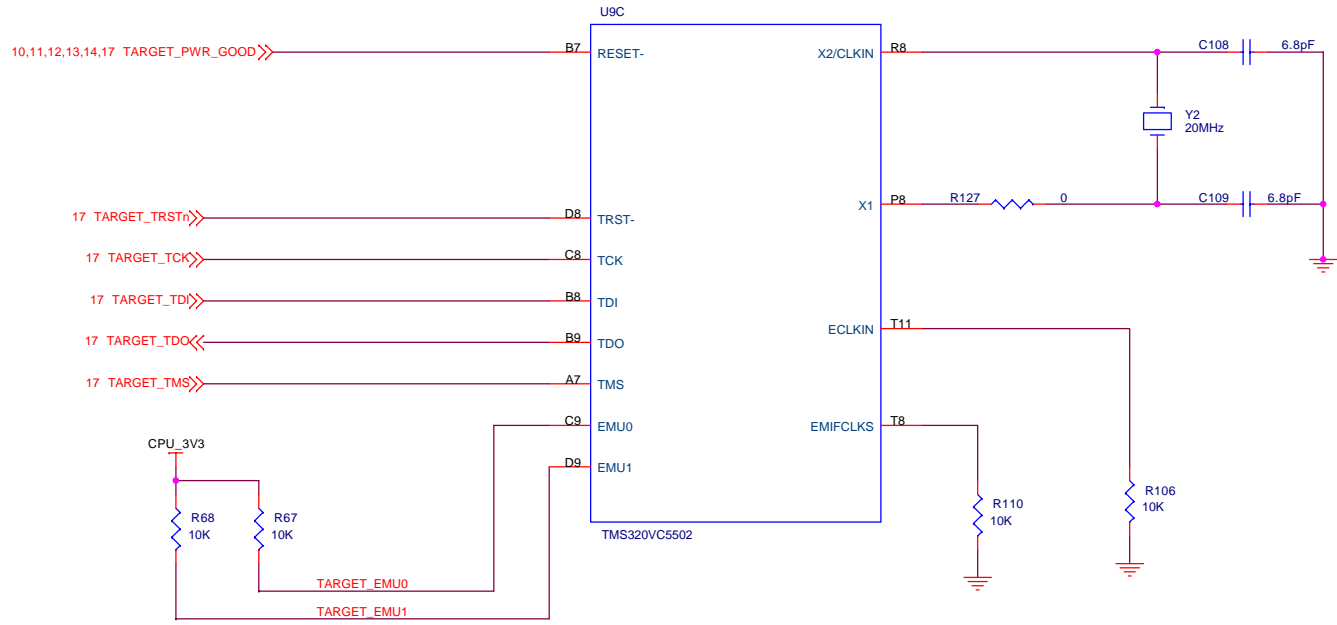
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CPU_3V3
 CPU_3V3 >>> CPU_3V3 2,5,6,10

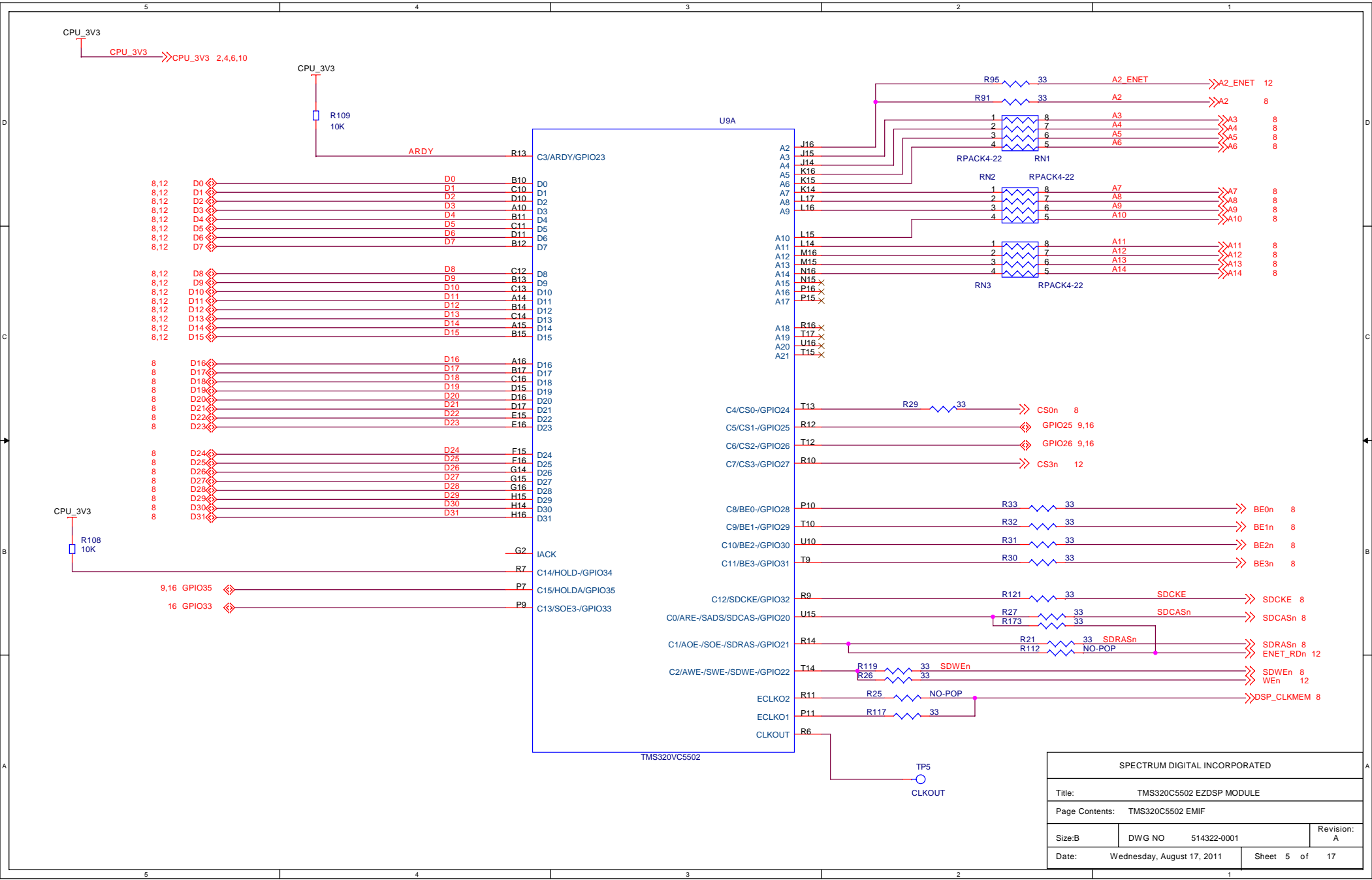
CORE CLOCK IS INPUT CLOCK DIVIDED BY
 DIVIDER D0 TIMES PLL

DIVIDER D0 = DIVIDE BY 1 TO 32

MULTIPLIER = TIMES 2 TO 15



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3.3 VOLTS AT 50mA

CPU_3V3

L7

BLM18AG601SN1D

1206

C94

C92

C88

C89

10uF

1uF

0.1uF

1000pF

DSP_DVDD

C35

C84

C90

C77

C65

10uF

0.1uF

0.1uF

0.1uF

0.1uF

C40

C57

C51

C58

C72

C80

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

DSP_CVDD

C86

C75

C91

C76

C67

C64

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

C111

C46

C50

C47

C62

C69

C85

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

1.26 VOLTS AT 240mA

VCC_1V26

VCC_1V26

VCC_1V26 <<VCC_1V26 10

CPU_3V3

CPU_3V3 <<CPU_3V3 2,4,5,10

U9D

TMS320VC5502

PVDD

DVDD.1

DVDD.2

DVDD.3

DVDD.4

DVDD.5

DVDD.6

DVDD.7

DVDD.8

DVDD.9

CVDD.1

CVDD.2

CVDD.3

CVDD.4

CVDD.5

CVDD.6

CVDD.7

CVDD.8

CVDD.9

CVDD.10

CVDD.11

NC,U8

VSS1

VSS2

VSS3

VSS4

VSS5

VSS6

VSS7

VSS8

VSS9

VSS10

VSS11

VSS12

VSS13

VSS14

VSS15

VSS16

VSS17

VSS18

VSS19

VSS20

VSS21

VSS22

VSS23

VSS24

VSS25

VSS26

VSS27

VSS28

VSS29

VSS30

VSS31

VSS32

VSS33

VSS34

VSS35

VSS36

VSS37

VSS38

VSS39

VSS40

VSS41

VSS42

G1

L1

P1

U6

U9

U11

U14

R17

N17

J17

G17

C17

A12

A9

A8

A3

U3

G7

G8

G9

G10

G11

H7

H8

H9

H10

H11

J7

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J11

K7

K8

K9

K10

K11

L7

L8

L9

L10

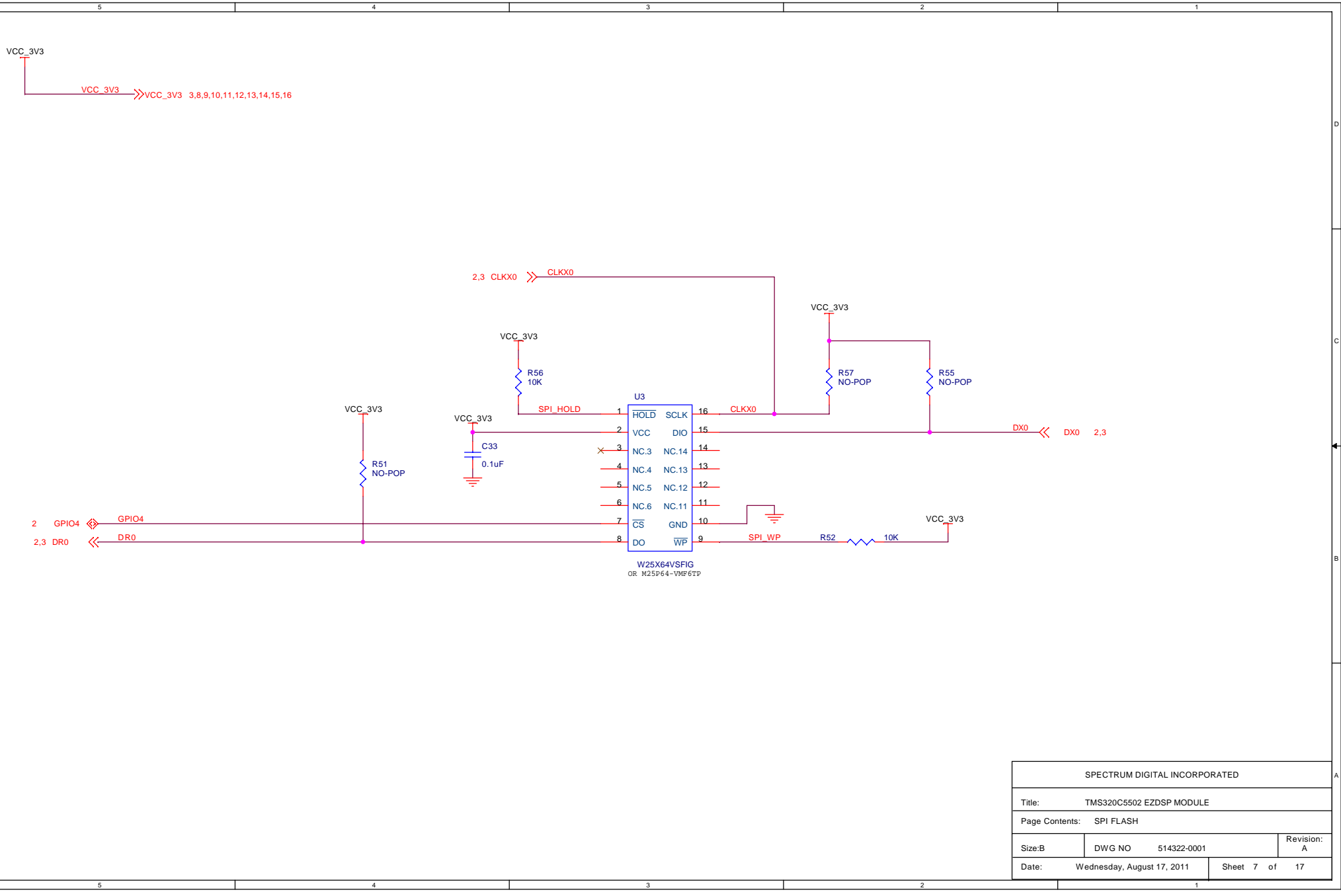
L11

TP1

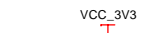
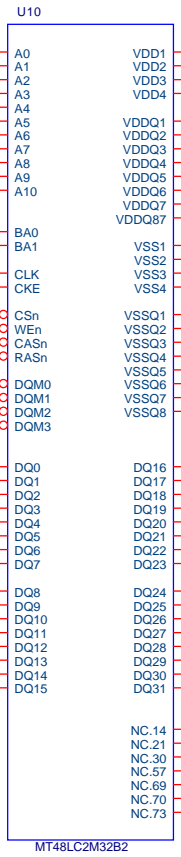
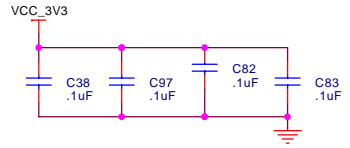
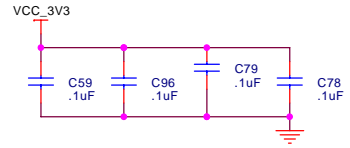
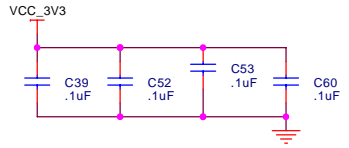
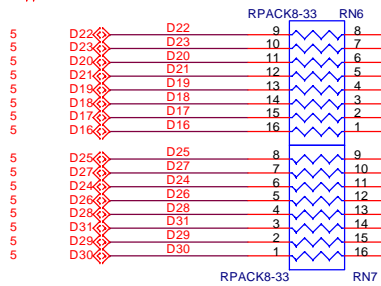
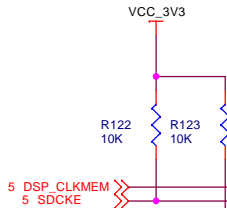
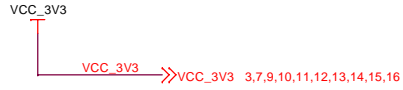
GND

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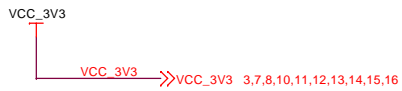
Title: TMS320C5502 EZDSP MODULE			
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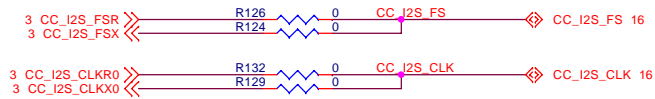
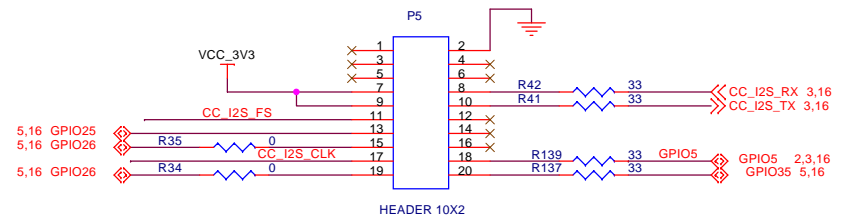
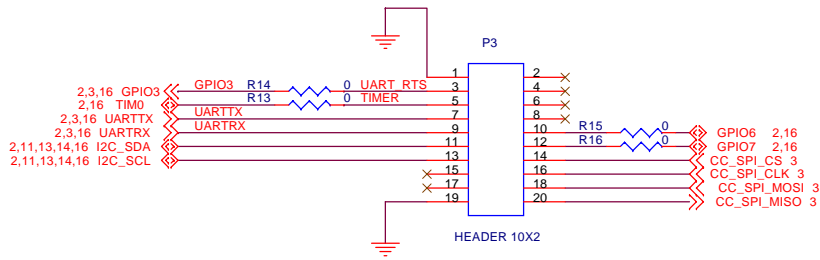
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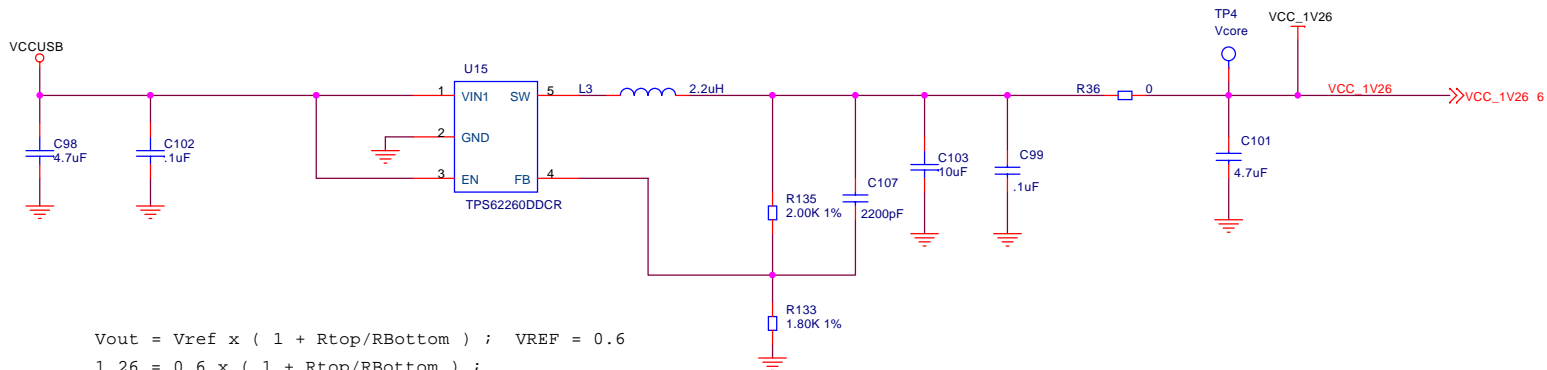
SPECTRUM DIGITAL INCORPORATED			
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NOTE: DIMENSIONS AND LOCATIONS OF THESE CONNECTORS MUST MEET SPECIFICATION FOR INTERFACE MODULES



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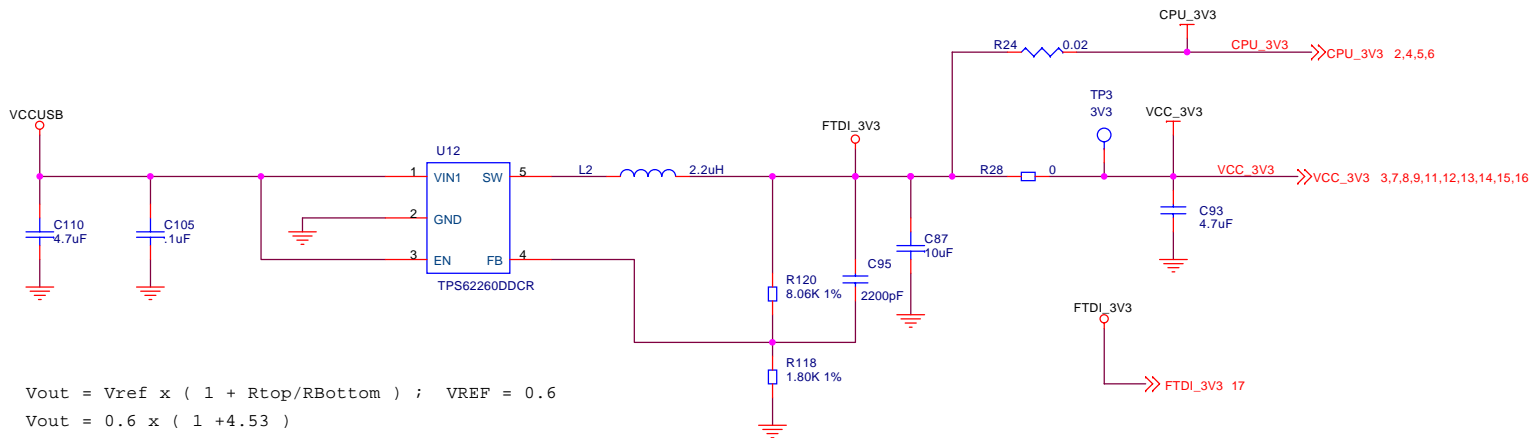


$$V_{out} = V_{ref} \times (1 + R_{top}/R_{bottom}) ; \quad V_{REF} = 0.6$$

$$1.26 = 0.6 \times (1 + R_{top}/R_{bottom}) ;$$

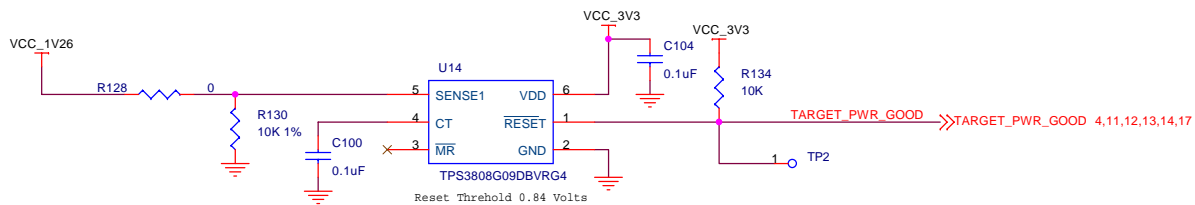
$$2.1 = (1 + R_{top}/R_{bottom}) ;$$

$$1.1 R_{bottom} = R_{top} ;$$

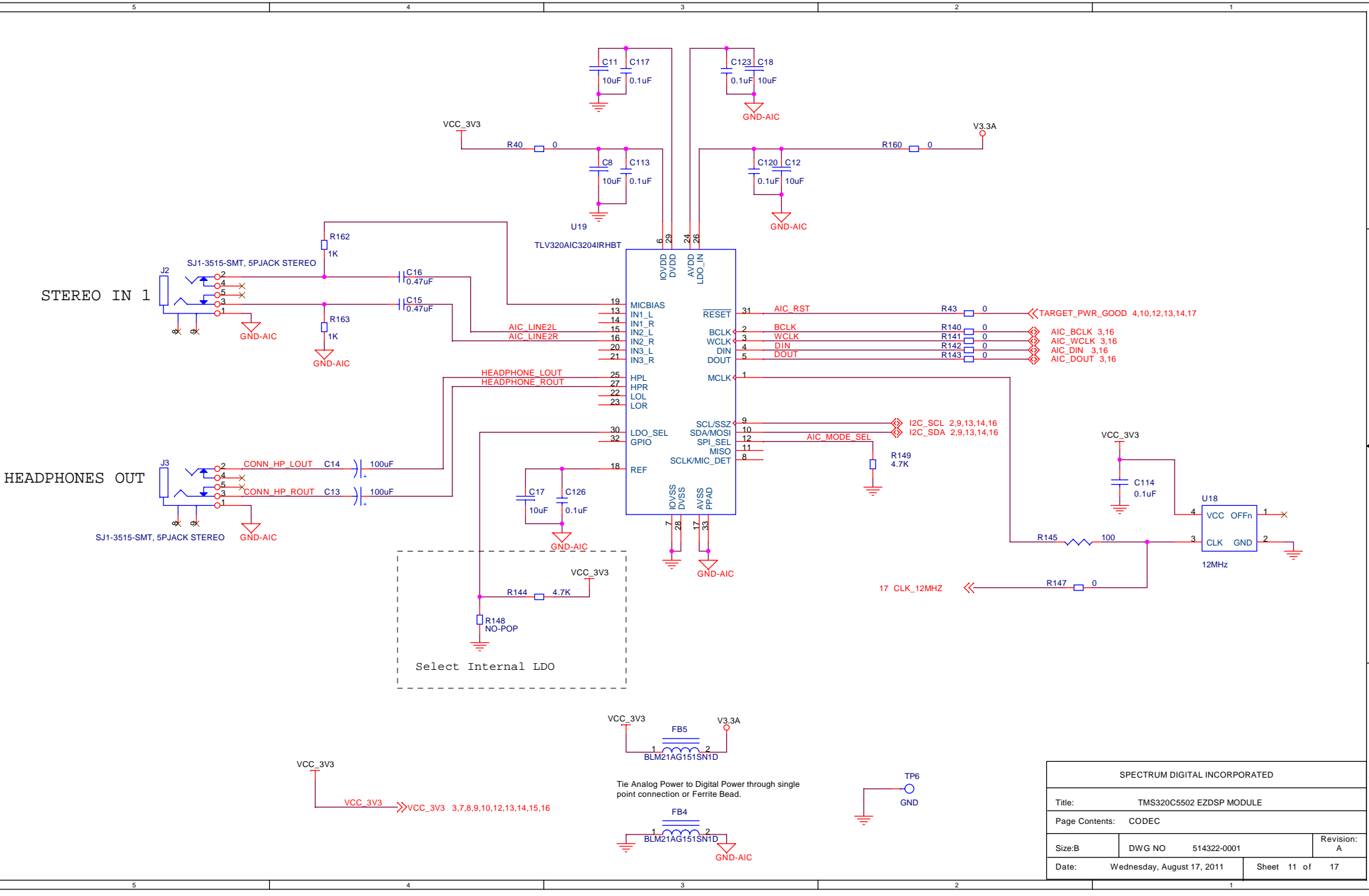


$$V_{out} = V_{ref} \times (1 + R_{top}/R_{bottom}) ; \quad V_{REF} = 0.6$$

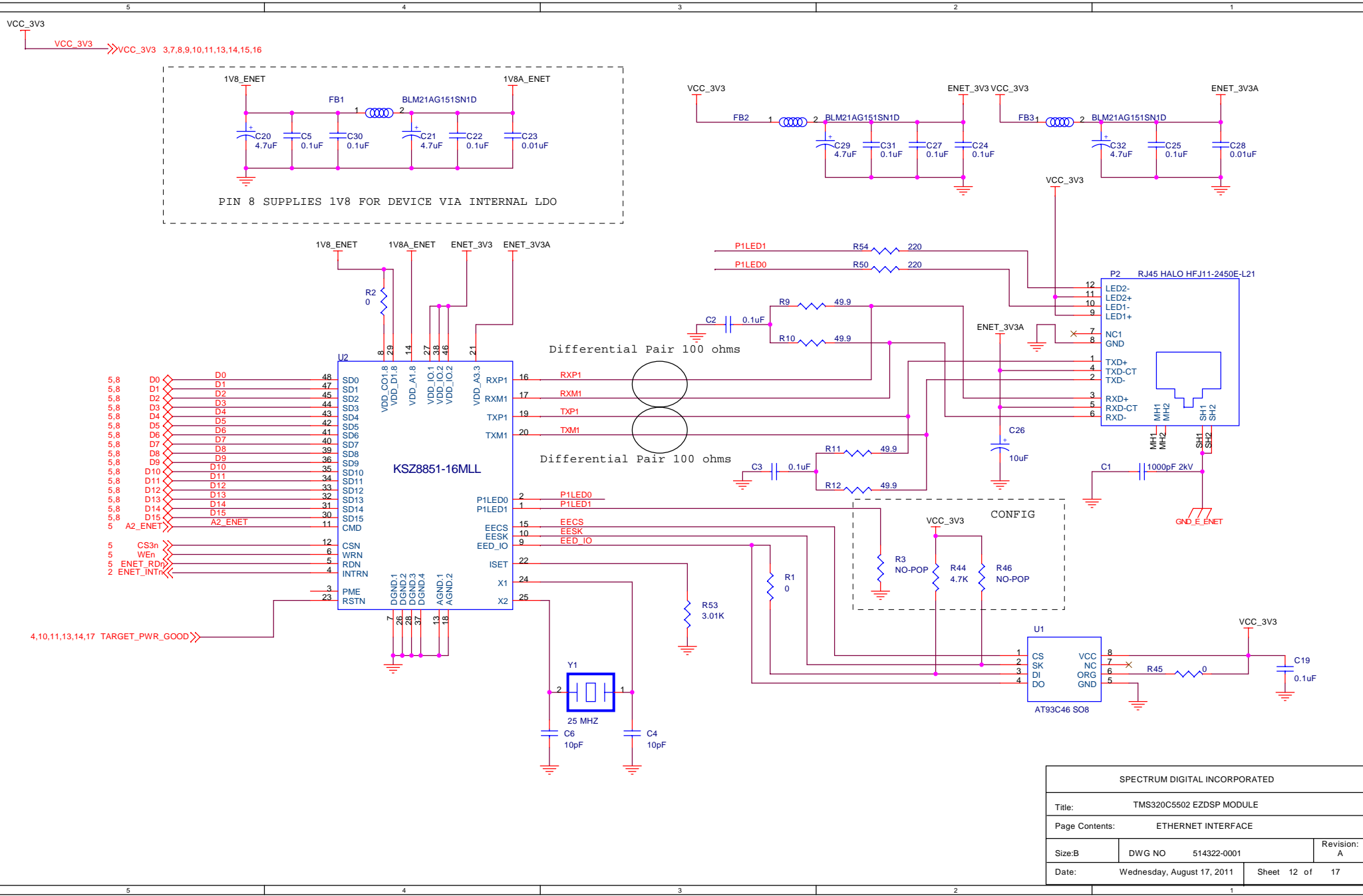
$$V_{out} = 0.6 \times (1 + 4.53)$$



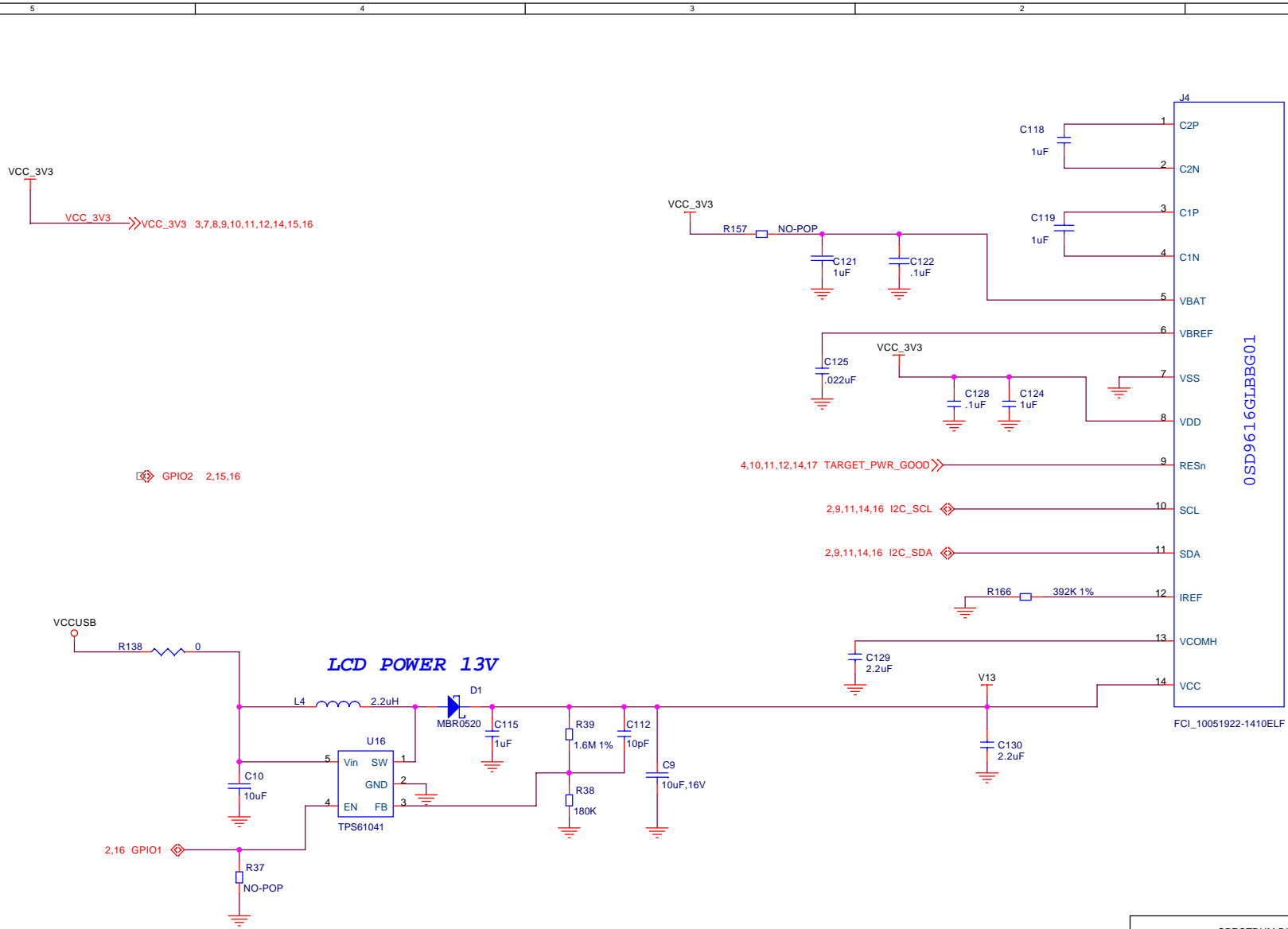
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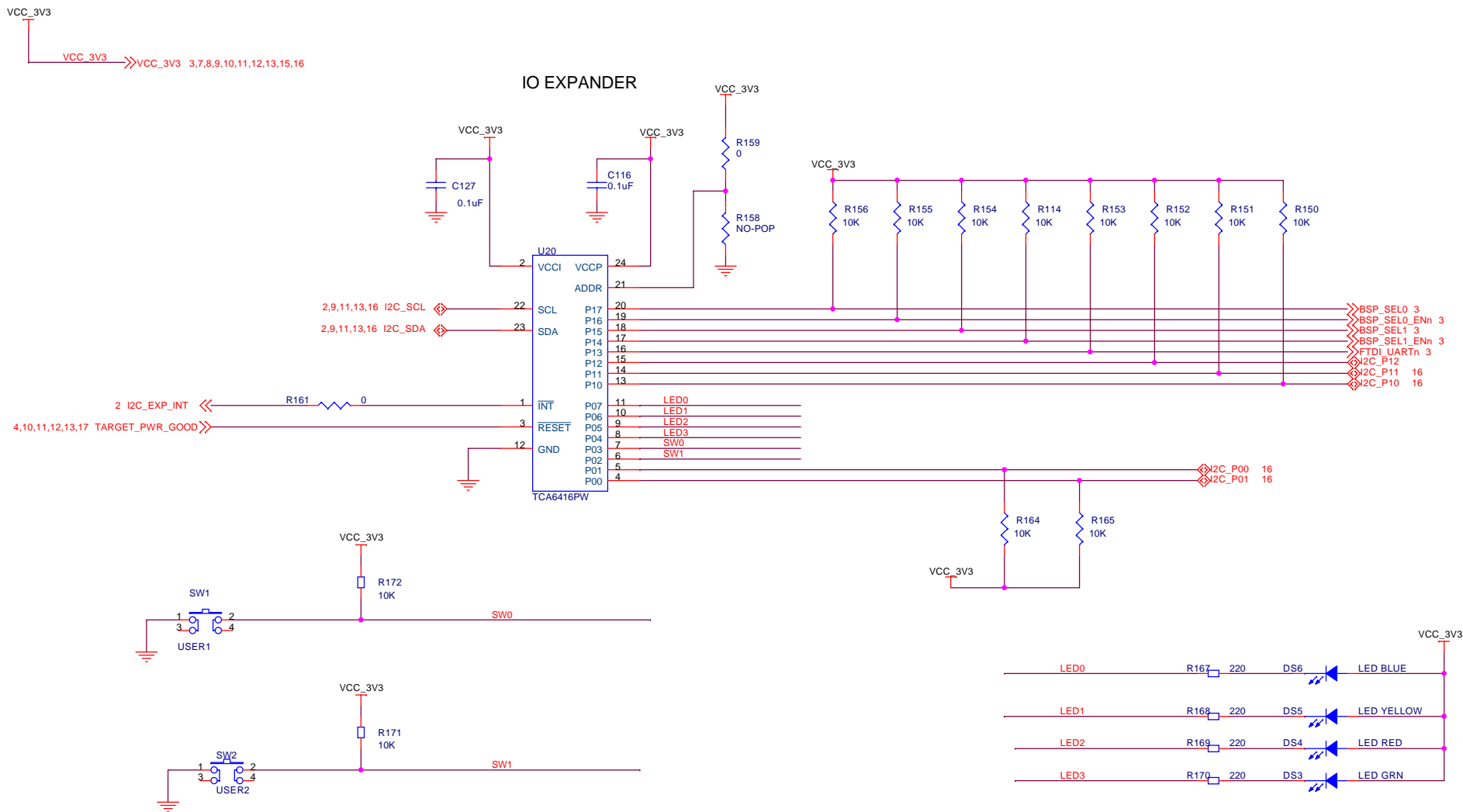
SPECTRUM DIGITAL INCORPORATED			
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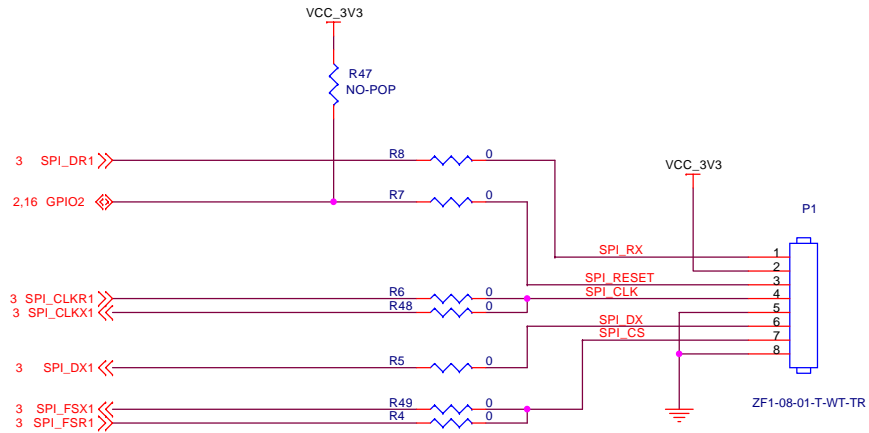


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Title		
<Title>		
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VCC_3V3
 VCC_3V3 >> VCC_3V3 3,7,8,9,10,11,12,13,14,16



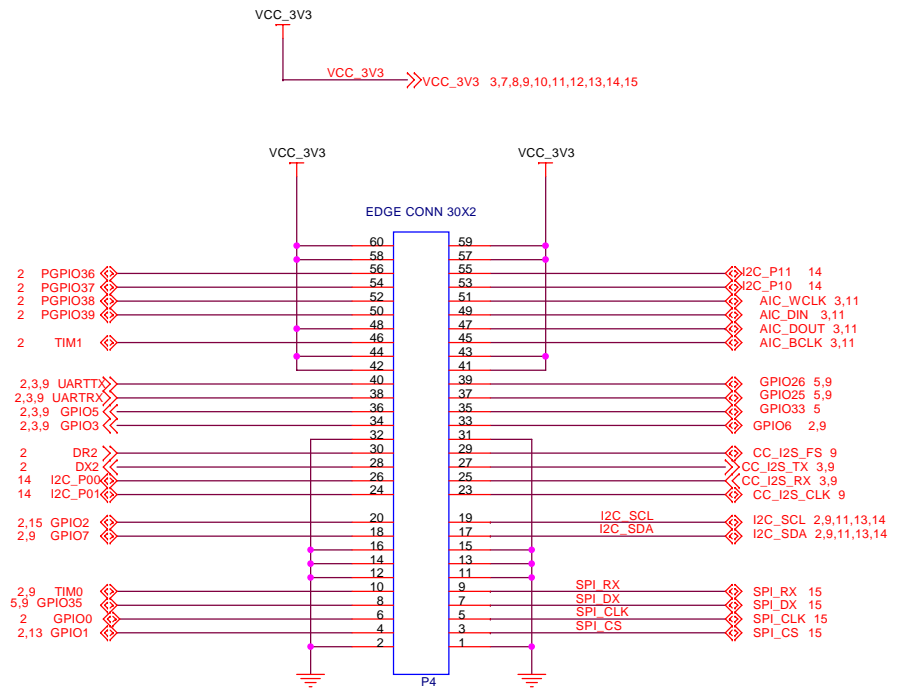
SPI_RX << SPI_RX 16

SPI_CLK << SPI_CLK 16

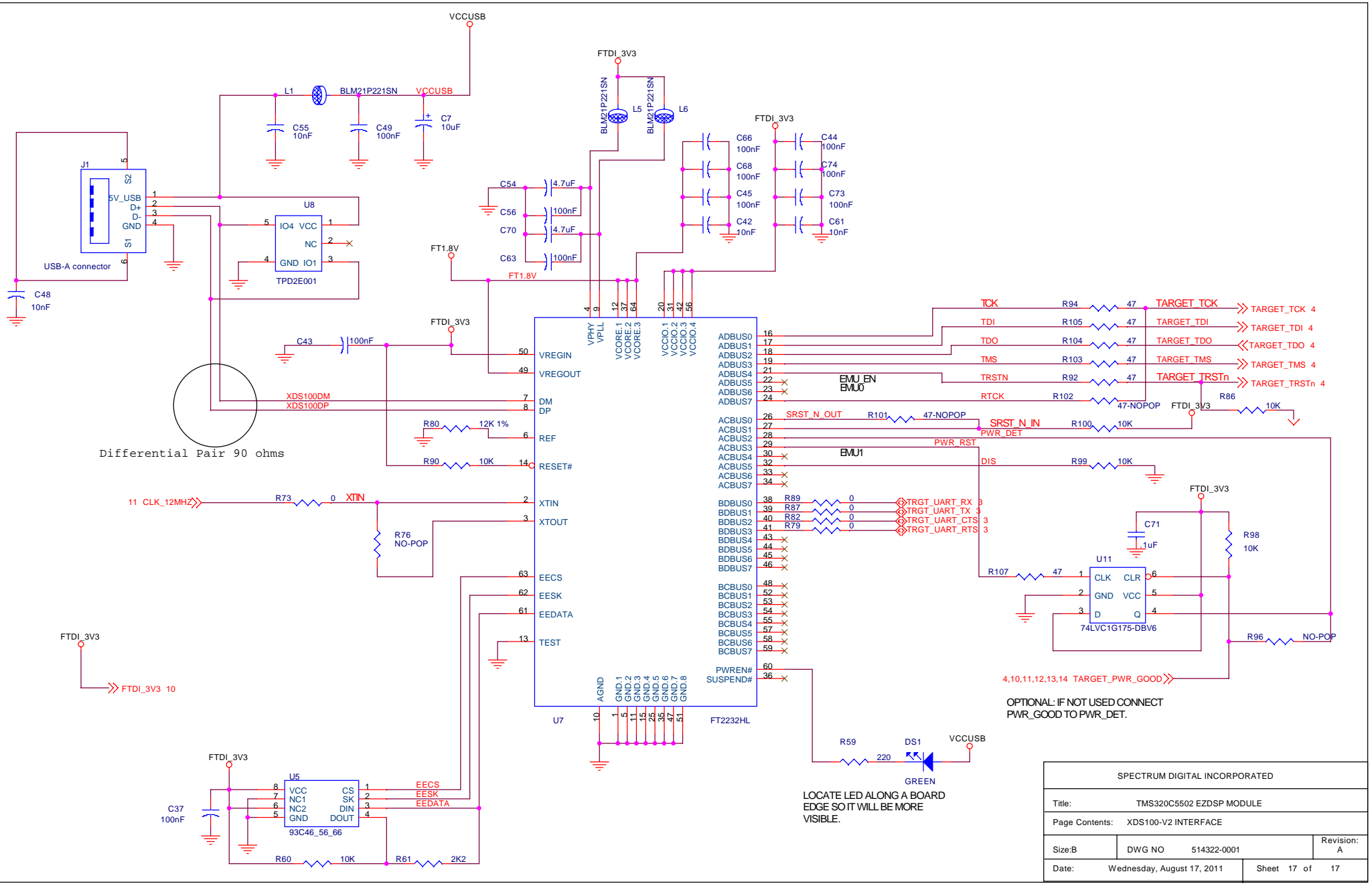
SPI_DX << SPI_DX 16

SPI_CS << SPI_CS 16

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Differential Pair 90 ohms

LOCATE LED ALONG A BOARD EDGE SO IT WILL BE MORE VISIBLE.

OPTIONAL: IF NOT USED CONNECT PWR_GOOD TO PWR_DET.

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