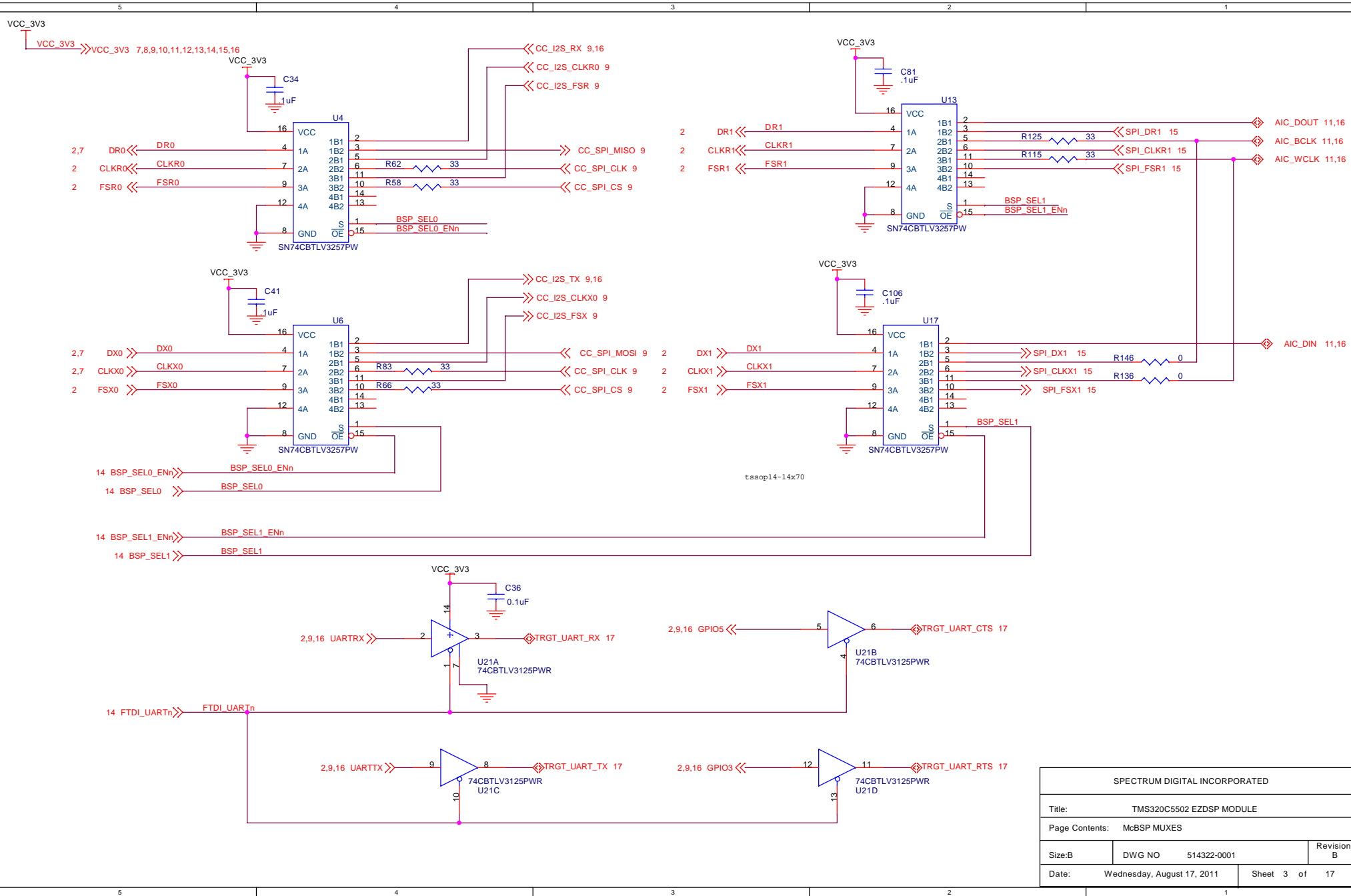


SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: GPIO,BSP,SPI,I2C			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet 2 of	17



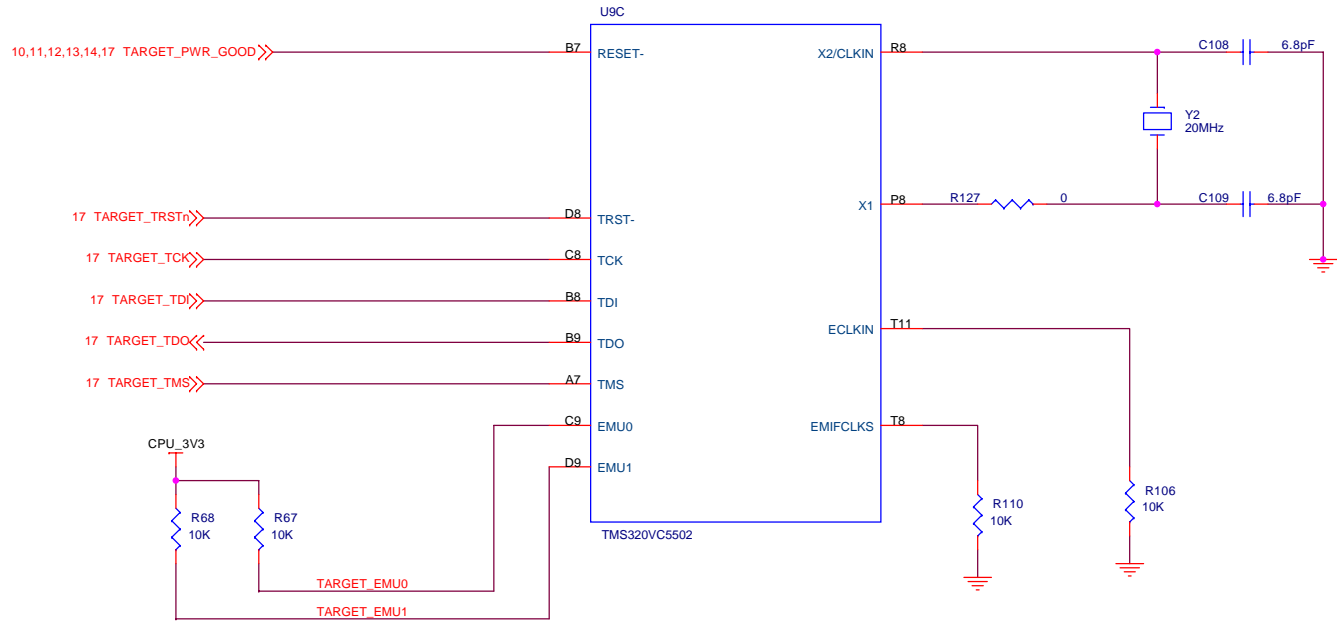
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Title: TMS320C5502 EZDSP MODULE			
Page Contents: McBSP MUXES			
Size: B	DWG NO	514322-0001	Revision: B
Date:	Wednesday, August 17, 2011	Sheet 3 of	17

CPU_3V3
 CPU_3V3 >>> CPU_3V3 2,5,6,10

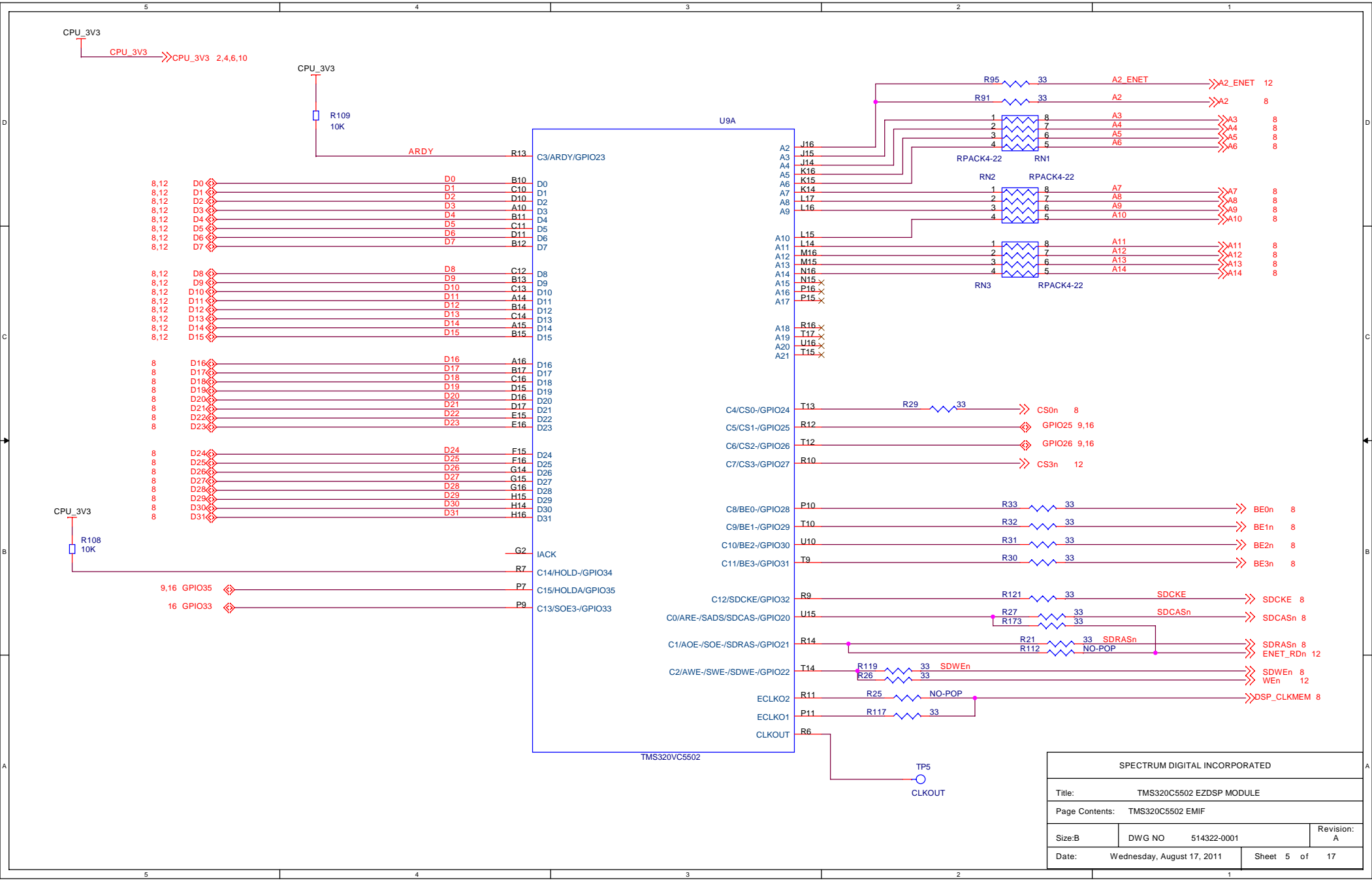
CORE CLOCK IS INPUT CLOCK DIVIDED BY
 DIVIDER D0 TIMES PLL

DIVIDER D0 = DIVIDE BY 1 TO 32

MULTIPLIER = TIMES 2 TO 15



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: CLOCK,JTAG,USB			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet 4 of	17



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 E2DSP MODULE			
Page Contents: TMS320C5502 EMIF			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011		Sheet 5 of 17

3.3 VOLTS AT 50mA

CPU_3V3

L7

BLM18AG601SN1D

1206

C94

C92

C88

C89

10uF

1uF

0.1uF

1000pF

DSP_DVDD

C35

10uF

C84

0.1uF

C90

C77

C65

10uF

0.1uF

0.1uF

0.1uF

0.1uF

C40

10uF

C57

0.1uF

C51

C58

C72

C80

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

DSP_CVDD

C86

10uF

C75

0.1uF

C91

0.1uF

C76

C67

C64

10uF

0.1uF

0.1uF

0.1uF

0.1uF

C111

10uF

C46

0.1uF

C50

0.1uF

C47

C62

C69

C85

10uF

0.1uF

0.1uF

0.1uF

0.1uF

0.1uF

VCC_1V26

1.26 VOLTS AT 240mA

VCC_1V26

VCC_1V26 <<VCC_1V26 10

CPU_3V3

CPU_3V3 <<CPU_3V3 2,4,5,10

U9D

TMS320VC5502

PVDD

F1 DVDD.1
N1 DVDD.2
U5 DVDD.3
U13 DVDD.4
P17 DVDD.5
K17 DVDD.6
E17 DVDD.7
A13 DVDD.8
A5 DVDD.9

F1 CVDD.1
J1 CVDD.2
M1 CVDD.3
U4 CVDD.4
U12 CVDD.5
M17 CVDD.6
H17 CVDD.7
F17 CVDD.8
A11 CVDD.9
A6 CVDD.10
A4 CVDD.11

NC.U8

VSS1 G1
VSS2 L1
VSS3 P1
VSS4 U6
VSS5 U9
VSS6 U11
VSS7 U14
VSS8 R17
VSS9 N17
VSS10 J17
VSS11 G17
VSS12 C17
VSS13 A12
VSS14 A9
VSS15 A8
VSS16 A3
VSS17 U3

VSS18 G7
VSS19 G8
VSS20 G9
VSS21 G10
VSS22 H7
VSS23 H8
VSS24 H8
VSS25 H9
VSS26 H10
VSS27 H11
VSS28 J7
VSS29 J8
VSS30 J9
VSS31 J10
VSS32 J11
VSS33 K7
VSS34 K8
VSS35 K9
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VSS39 L8
VSS40 L9
VSS41 L10
VSS42 L11

TP1

GND

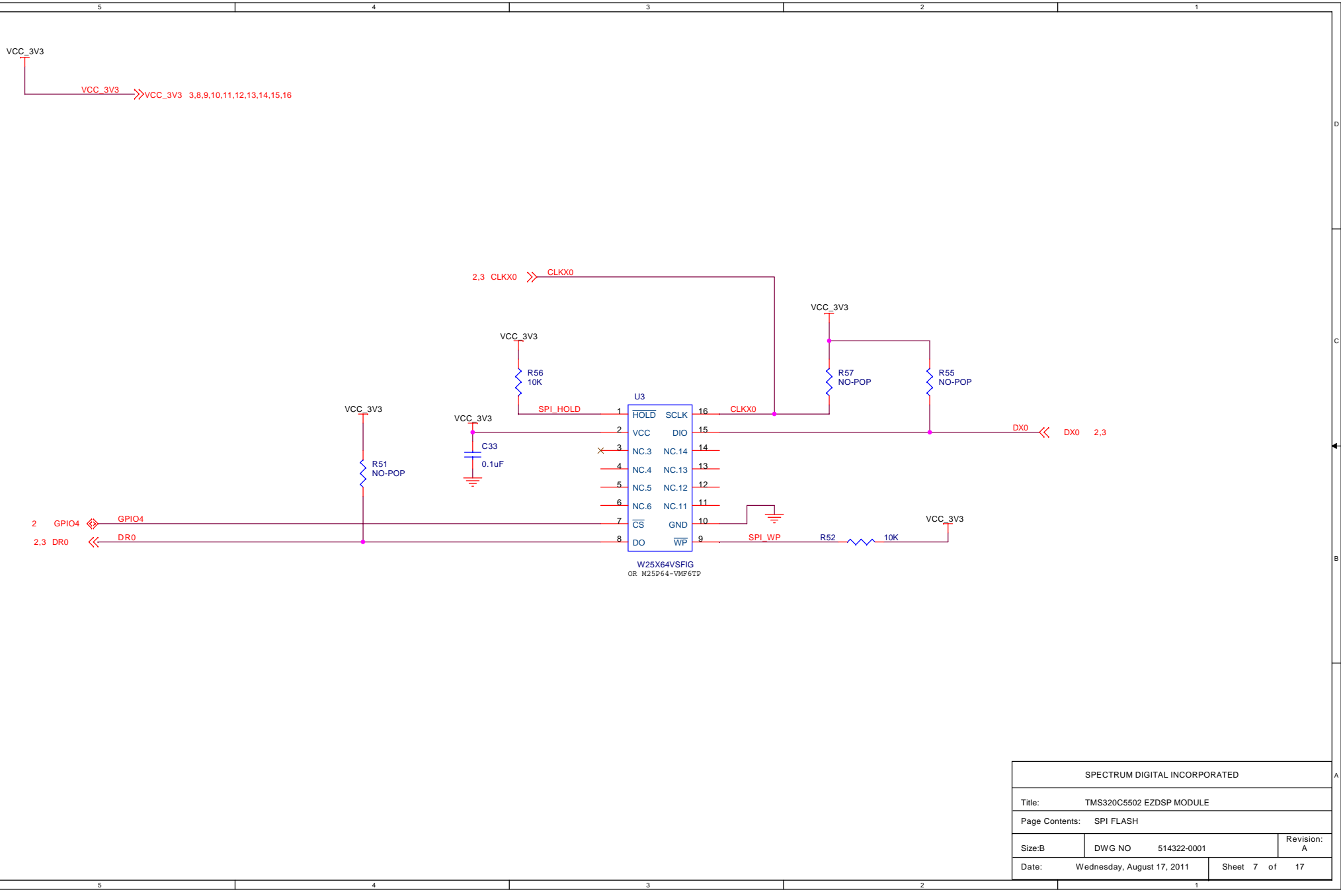
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Title: TMS320C5502 EZDSP MODULE

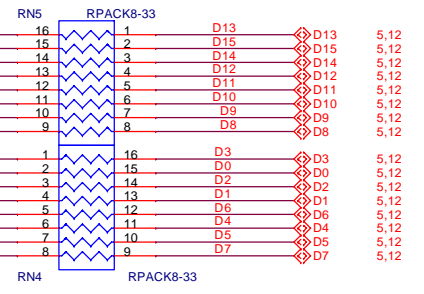
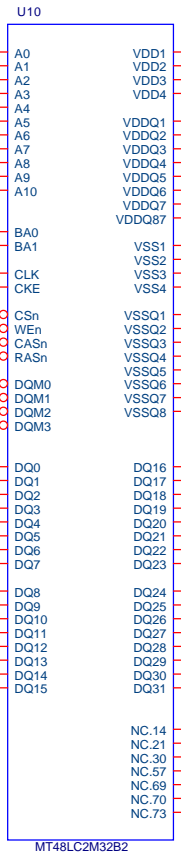
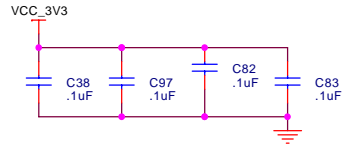
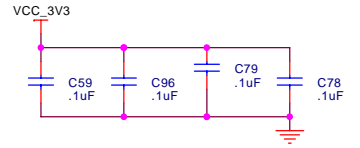
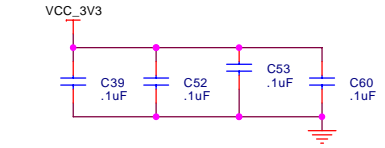
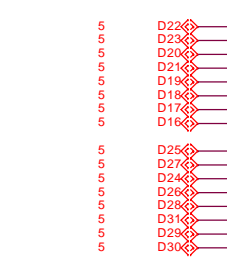
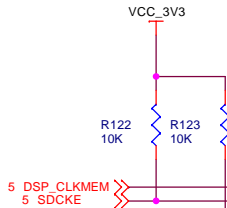
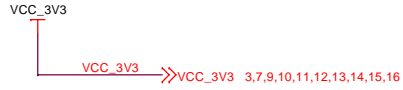
Page Contents: TMS320C5502 POWER

Size: B DWG NO: 514322-0001 Revision: A

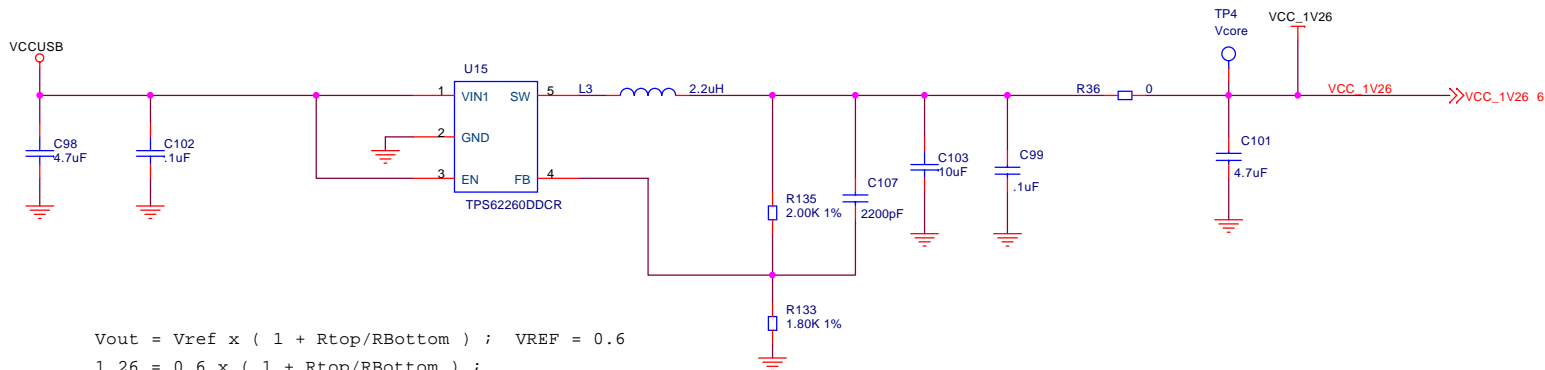
Date: Wednesday, August 17, 2011 Sheet 6 of 17



SPECTRUM DIGITAL INCORPORATED		
Title: TMS320C5502 EZDSP MODULE		
Page Contents: SPI FLASH		
Size: B	DWG NO 514322-0001	Revision: A
Date: Wednesday, August 17, 2011	Sheet 7 of 17	



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: SDRAM			
Size: B	DWG NO: 514322-0001	Revision: A	
Date: Wednesday, August 17, 2011	Sheet 8 of 17		

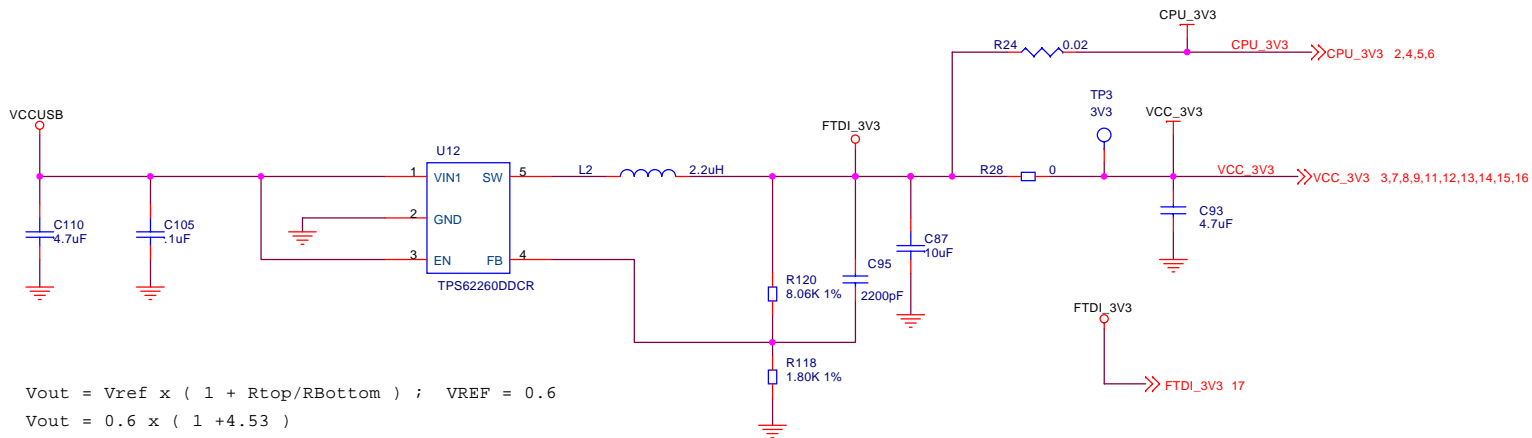


$$V_{out} = V_{ref} \times (1 + R_{top}/R_{bottom}) ; \quad V_{REF} = 0.6$$

$$1.26 = 0.6 \times (1 + R_{top}/R_{bottom}) ;$$

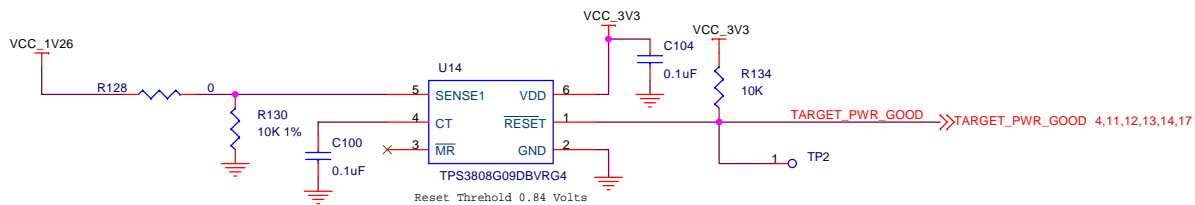
$$2.1 = (1 + R_{top}/R_{bottom}) ;$$

$$1.1 R_{bottom} = R_{top} ;$$

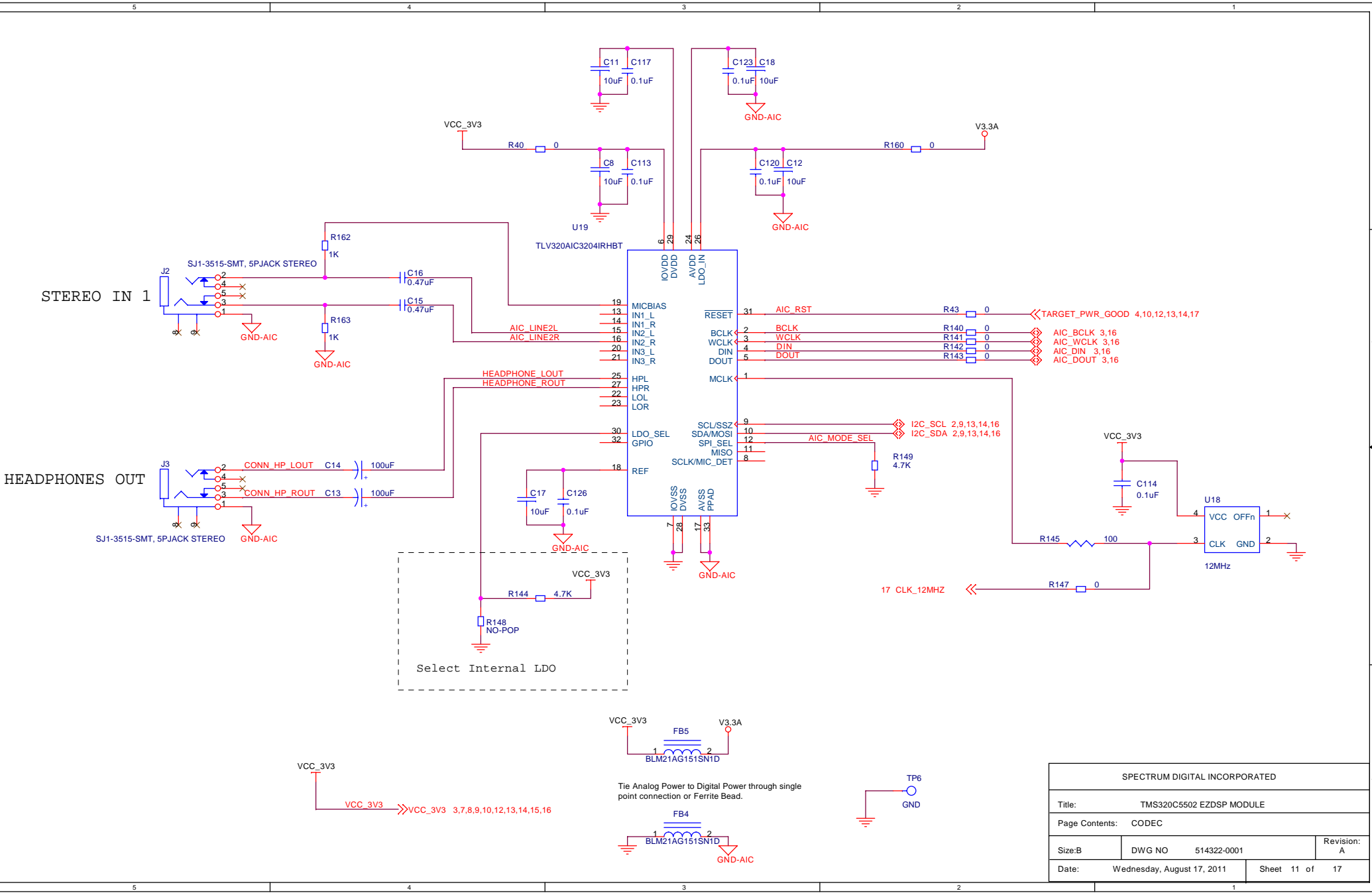


$$V_{out} = V_{ref} \times (1 + R_{top}/R_{bottom}) ; \quad V_{REF} = 0.6$$

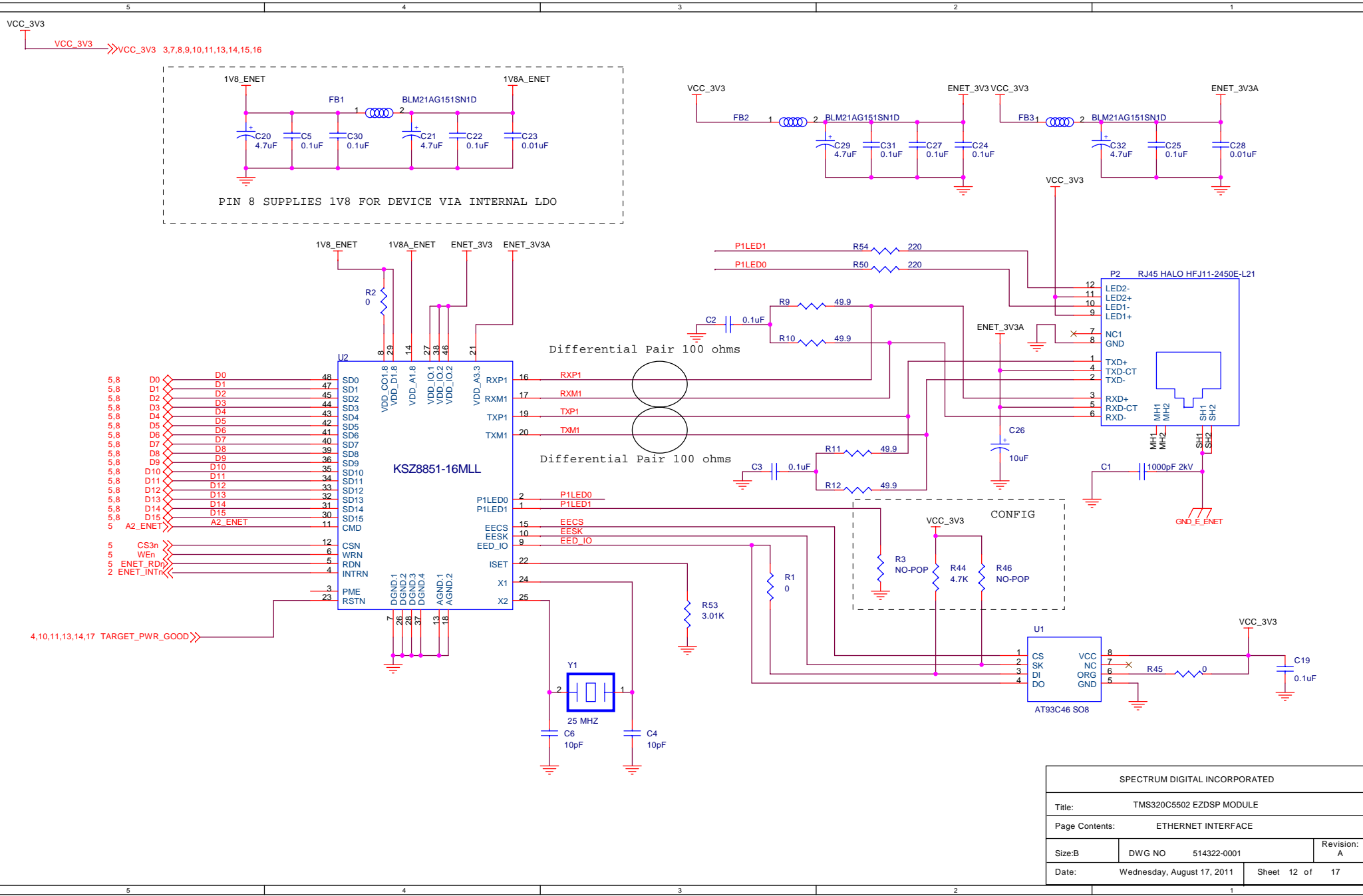
$$V_{out} = 0.6 \times (1 + 4.53)$$



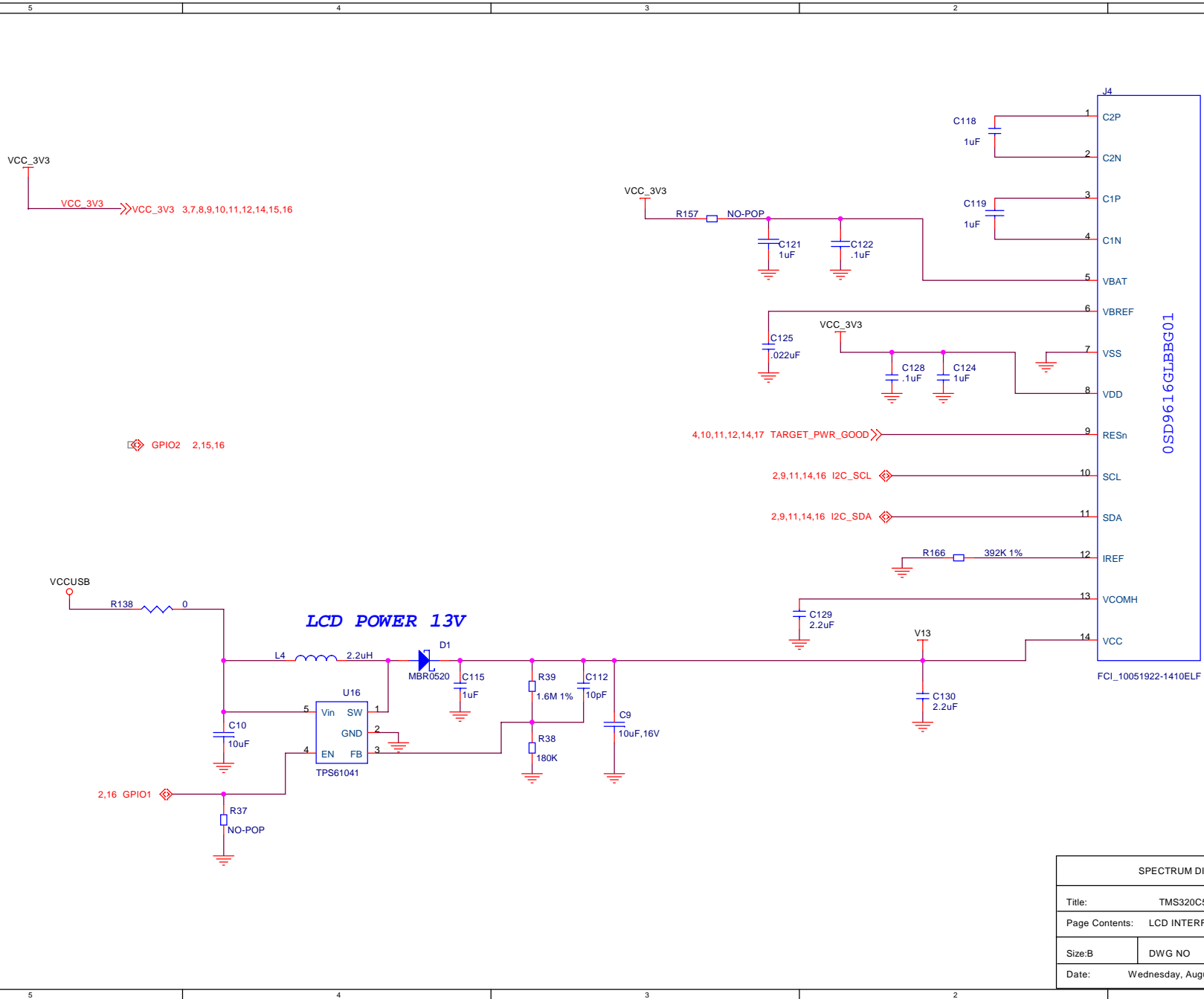
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: POWER MANAGEMENT			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Thursday, September 01, 2011	Sheet	10 of 17



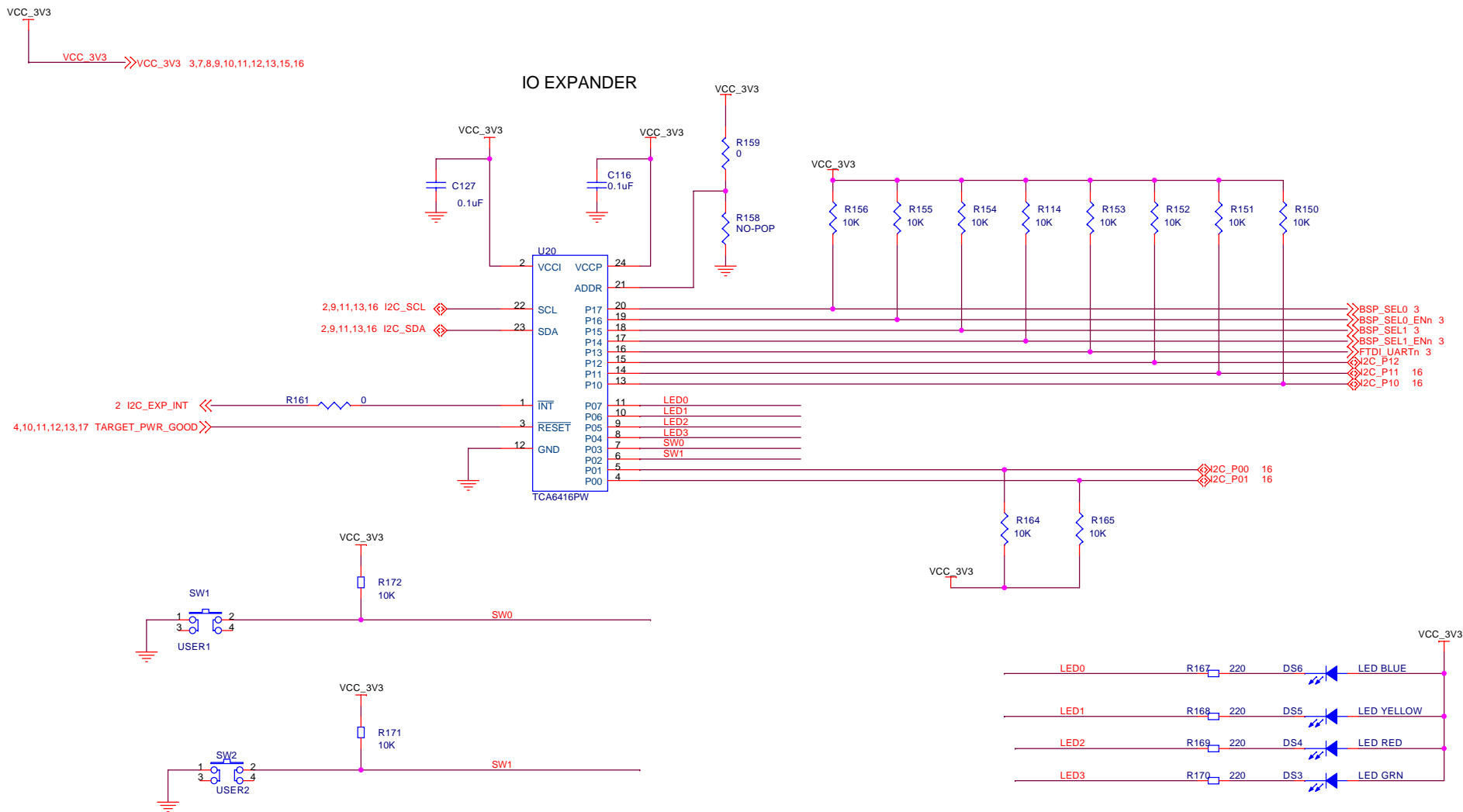
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Title: TMS320C5502 EZDSP MODULE			
Page Contents: CODEC			
Size: B	DWG NO: 514322-0001	Revision: A	
Date: Wednesday, August 17, 2011	Sheet 11 of 17		



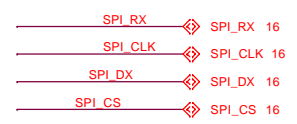
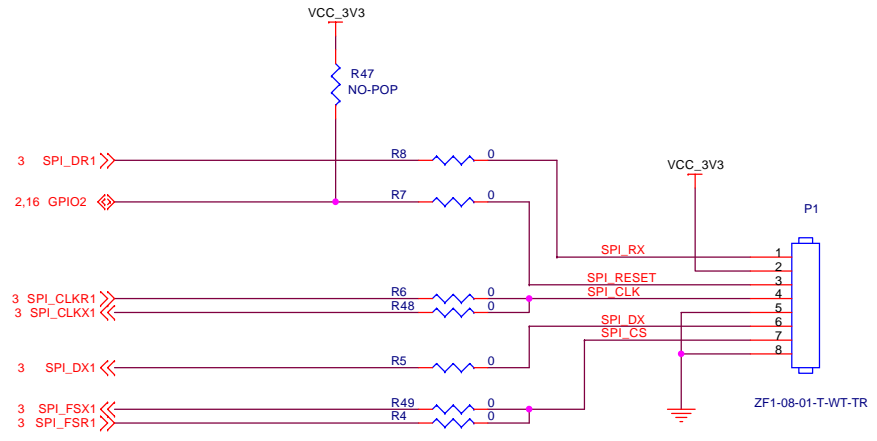
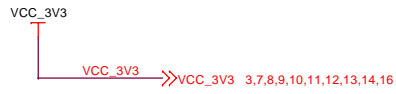
SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: ETHERNET INTERFACE			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet 12 of	17



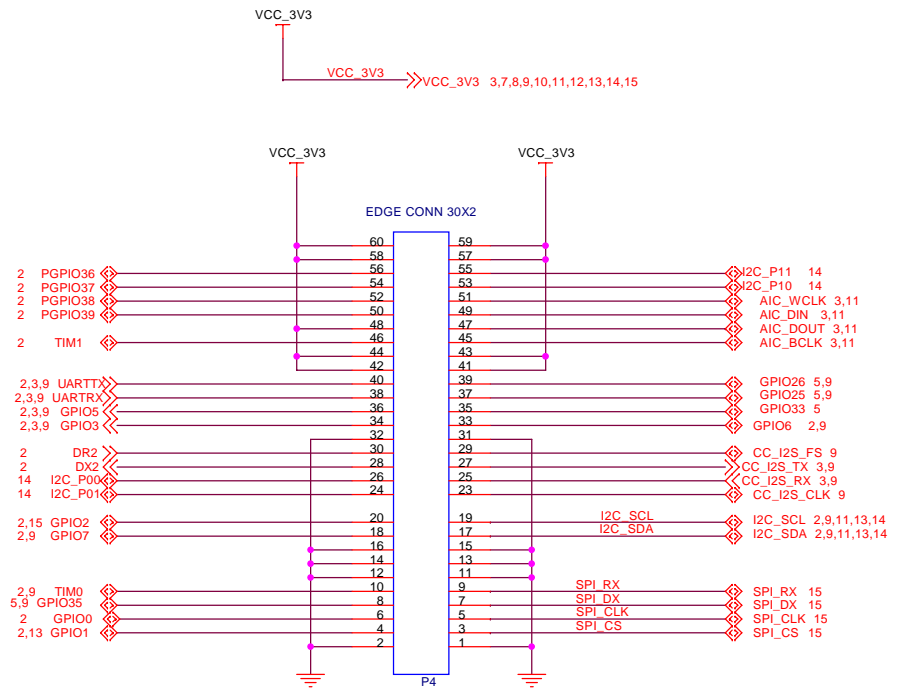
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Title: TMS320C5502 EZDSP MODULE			
Page Contents: LCD INTERFACE			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet	13 of 17



Title		
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Size	Document Number	Rev
B	<Doc>	<RevC>
Date:	Wednesday, August 17, 2011	Sheet 14 of 17



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: FINGER PRINT CONNECTOR			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet 15 of	17



SPECTRUM DIGITAL INCORPORATED			
Title: TMS320C5502 EZDSP MODULE			
Page Contents: EXPANSION CONNECTORS			
Size: B	DWG NO	514322-0001	Revision: A
Date:	Wednesday, August 17, 2011	Sheet 16 of	17

